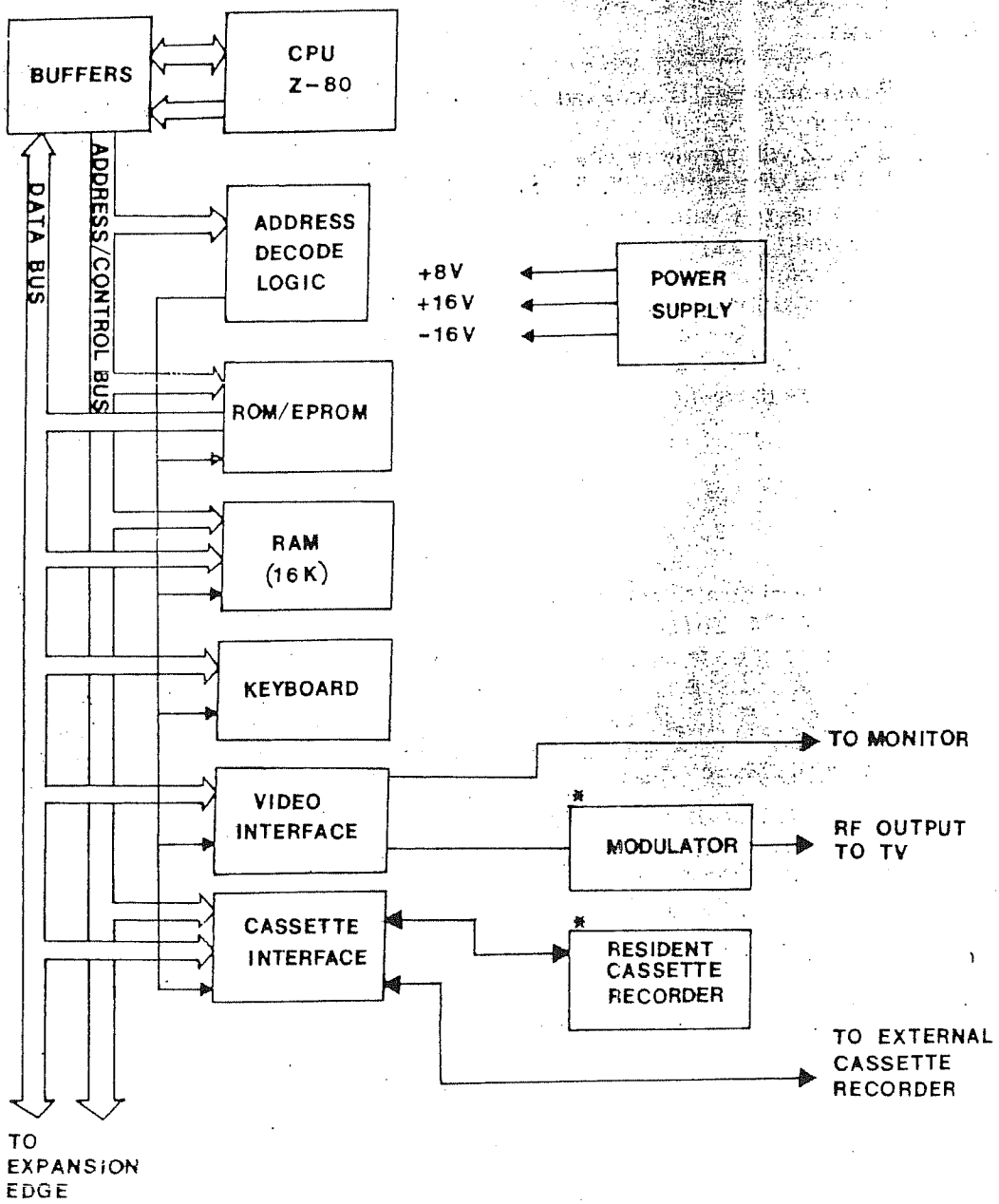
TABLE OF CONTENTS

1. THEORY OF OPERATION

The hardware of the GENIE system is described one-by-one in this section. The GENIE consists of the following functional blocks: CPU, system ROM, user RAM, address decode and buffers, video interface, cassette interface, keyboard and power supply. These blocks are generally common to both GENIE I (EG3003) and GENIE II (EG3008), and the differences will be mentioned in the appropriate sections. See Fig. 1.1 on system blocks.

Fig. 1.1 SYSTEM BLOCK DIAGRAM



* NOTE: This is absent in GENIE II

1.1 CPU

Z-80 is employed as the CPU chip which is an 8-bit N-channel microprocessor with 16 address lines. This 40-pin LSI requires single +5V DC supply. It provides 158 software instructions including those of 8080A CPU. Details refer to the data sheet of Z-80 in the appendix and the technical manual of Z-80.

1.1.1 Clock

The CPU operates at 1.77 MHz. derived from a crystal oscillator of 10.644 MHz and a divide-by-six counter, Z38. The oscillator is implemented on the interface board with three inverters of Z31 and a 10.644 MHz crystal.

1.1.2 Reset

Power-on reset and system reset are provided for proper operation of the GENIE. Power-on reset is achieved by a RC delay circuit. Initially, the capacitor C2 is discharged through a diode D1 as +5V DC is turned OFF. Once +5V DC is switched ON, C2 will slowly be charged up towards +5V. Pin 26 of Z-80 will experience a logic LOW as Vcc of the CPU has reached the operating supply voltage. Then, the CPU will be initialized with program counter set to ØØØØH, and all information stored will be lost when the system starts execution at location zero.

System reset is done by pulling LOW the input of $\overline{\text{NMI}}$ (pin 17 of Z-80). As $\overline{\text{NMI}}$ (non-maskable interrrupt) is active LOW, the CPU will re-start execution at location ØØ66H without altering the programs stored in memory. The system reset button is present on the back panel of the GENIE. A capacitor C1 is added across the switch to minimize the switch bounce.

1.1.3 Buses

The bi-directional data lines from the CPU are immediately buffered by Z18, Z19, and Z20 (74L367). The input buffers are enabled when either $\overline{\text{M1}}$ or $\overline{\text{RD}}$ is active LOW during op code fetch, interrupt acknowledge, memory read or input cycles. The output buffers are disabled when the control signal, $\overline{\text{ADDBS}}/\overline{\text{DODBS}}$ is LOW.

The 16 unidirectional address lines are also buffered by Z4, Z6 and Z17 (74LS367). These address lines can be isolated from the system bus by pulling $\overline{\text{ADDBS}}/\overline{\text{DODBS}}$ LOW.

The control lines for read/write and input/output are buffered by Z16 (74LS367), and are decoded by Z15 to get memory read/write ($\overline{\text{MRD}}$ and $\overline{\text{MWR}}$) and port input/output ($\overline{\text{IN}}$ and $\overline{\text{OUT}}$) control signals. These control lines can be disabled by making $\overline{\text{C}}/\overline{\text{CDBS}}/\overline{\text{STADBS}}$ LOW.

1.1.4 Address Decode

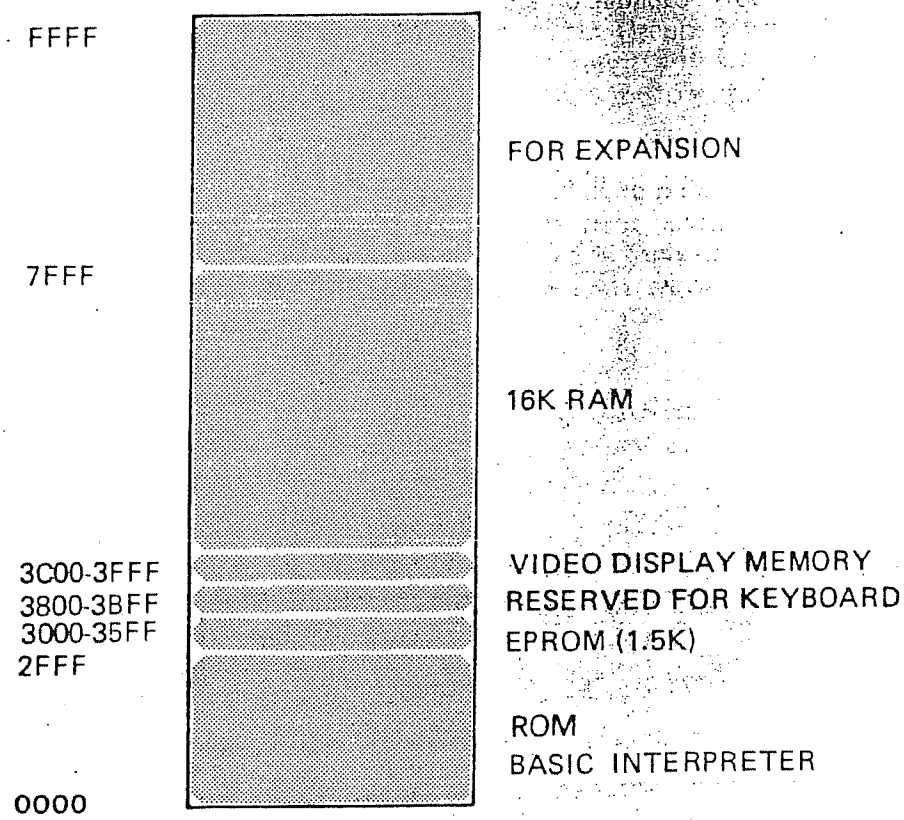
The address decode logic enables the CPU to access ROM, RAM, keyboard and video interface respectively. The logic is formed by Z22, Z25, Z35 and Z21. The decode scheme is illustrated as follows:

A15	A14	A13	A12	A11	A10	ENABLE	DECODED OUTPUT
0	0	0	0	X	X	ROM1 (Z10)	Z22 pin 9, 10
0	0	0	1	X	X	ROM 2 (Z11)	Z22 pin 11, 12
0	0	1	0	X	X	ROM3 (Z12)	Z22 pin 6, 7
0	0	1	1	0	X	EPROM (Z13)	Z22 pin 5
0	0	1	1	1	0	Keyboard	Z35 pin 11
0	0	1	1	1	1	Video RAM	Z35 pin 3
0	1	X	X	X	X	16K RAM	Z35 Pin 11

Note: X means don't care.

Fig. 1.2 MEMORY MAP

MEMORY MAP



I/O PORT ASSIGNMENT

CASSETTE INTERFACE – FF, FE
PRINTER INTERFACE – FD

1.2 ROM

Both GENIE I and GENIE II have 12K bytes of Microsoft Extended BASIC interpreter stored in three 4K x 8 ROM's, E3001, E3002 and E3003. These ROM's are pin-compatible to standard 4K x 8 ROM chips. There is a 2K x 8 EPROM (2716) providing some special routines. In GENIE I, the extneded functions include upper case and lower case characters, flashing cursor, auto-repeat keyboard, screen print, machine language monitor and renumbering. It occupies 1.5K bytes of the EPROM.

In GENIE II, besides the upper case and lower case characters, auto-repeat keys, flashing cursor and screen print functions, the extra routines provide two more features. They are a dumb terminal, HOST communication, and RS232 communication routines. These routines occupy 1.5K bytes of the EPROM. How to use these routines is detailed in the User's manual of GENIE I and II.

The ROM's and EPROM share the data buffers (Z9) with the user RAM's. Z25 gives proper chip selection signals to these ROM's. When the ROM and EPROM are addressed, pin 11 of Z25 will be logic HIGH and disable the RAM select signal, $\overline{CAS}$ from Z37 pin 13. Conversely when the RAM's are addressed, pin 12 of Z25 becomes logic HIGH and pin 11 of Z25 logic LOW, that is, the ROM select decoder, Z22 is disabled.

1.3 RAM

Z-80 is capable of easily interfacing to dynamic RAM's. The control signal, $\overline{MREQ}$ (Memory Request) facilitates the addressing and refresh of dynamic RAM. Both GENIE I and II have 16K bytes of RAM's which are 4116 with access time of 250 nsec. They need power supply of +5V DC, +12V DC and −5V DC.

1.3.1 Generation of $\overline{RAS}$, MUX and $\overline{CAS}$

Other than Read/Write control, $\overline{RAS}$ (Row Address Strobe), MUX (Address multiplexing) and $\overline{CAS}$ (Column Address Strobe) are the essential control signals to the RAM array. $\overline{RAS}$ is the same signal as $\overline{MREQ}$. MUX and $\overline{CAS}$ are generated as in Fig. 1.3.

Fig. 1.3a $\overline{RAS}$, MUX AND $\overline{CAS}$

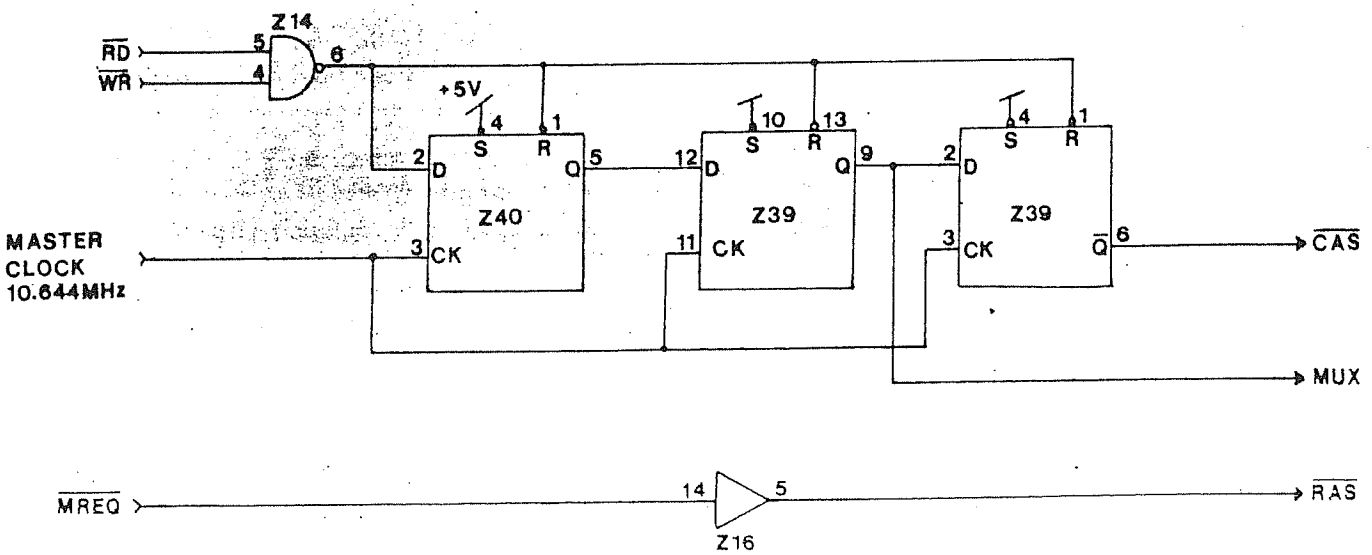
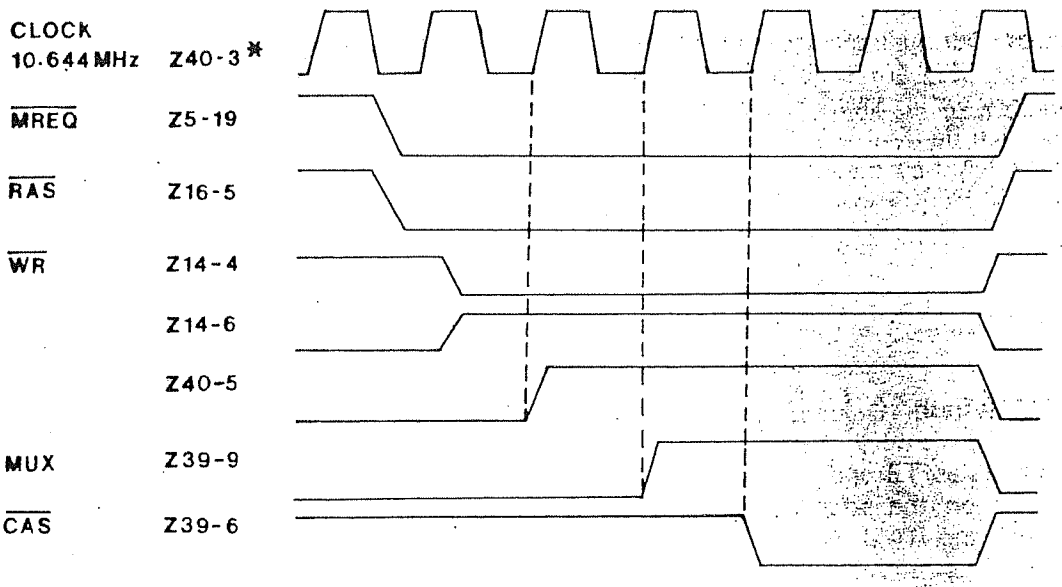


Fig. 1.3b TIMINGS OF $\overline{RAS}$, MUX AND $\overline{CAS}$



*NOTE: Z40-3 means pin 3 of Z40.

The generation of MUX and $\overline{CAS}$ is initiated and terminated by the $\overline{WR}$ or $\overline{RD}$ timing (Z14), and the active pulse width is determined by the time period of the master clock. When either $\overline{RD}$ or $\overline{WR}$ is active LOW, Z14-6 and Z40-2 will encounter a logic HIGH, and the D-type F/F (Z40-5) will change state from Ø to 1 upon the rising edge of the CLOCK. Then, MUX and $\overline{CAS}$ will become active at the following clocking edges respectively as shown in Fig. 1.3b.

1.3.2 Memory Read/Write

Since the RAM 4116 has internal row/column address latches, the address lines to the RAM are multiplexed by Z23 and Z24 (74LS157), and are controlled by the signal MUX. The row (or low order) address will appear on the address inputs of the RAM as MUX is LOW, and will be latched into the RAM by $\overline{RAS}$. As MUX is HIGH, the column (or high order) address appear on the address inputs of the RAM, and will be latched into the RAM by $\overline{CAS}$.

The addressing is similar in case of memory read and memory write although the strobe $\overline{CAS}$ appears earlier during memory read cycles than during memory write cycles. During memory read, $\overline{MWR}$ at pin 3 of 4116 is HIGH, and the data output buffers (Z9) are enabled. The stored data will be put onto the data bus. During memory write, $\overline{MWR}$ becomes LOW, $\overline{MRD}$ becomes HIGH, and the output buffer (Z9) will then be disabled. The information on the data bus will be strobed into the register of the RAM by the falling edge of $\overline{CAS}$.

1.3.3 RAM Refresh

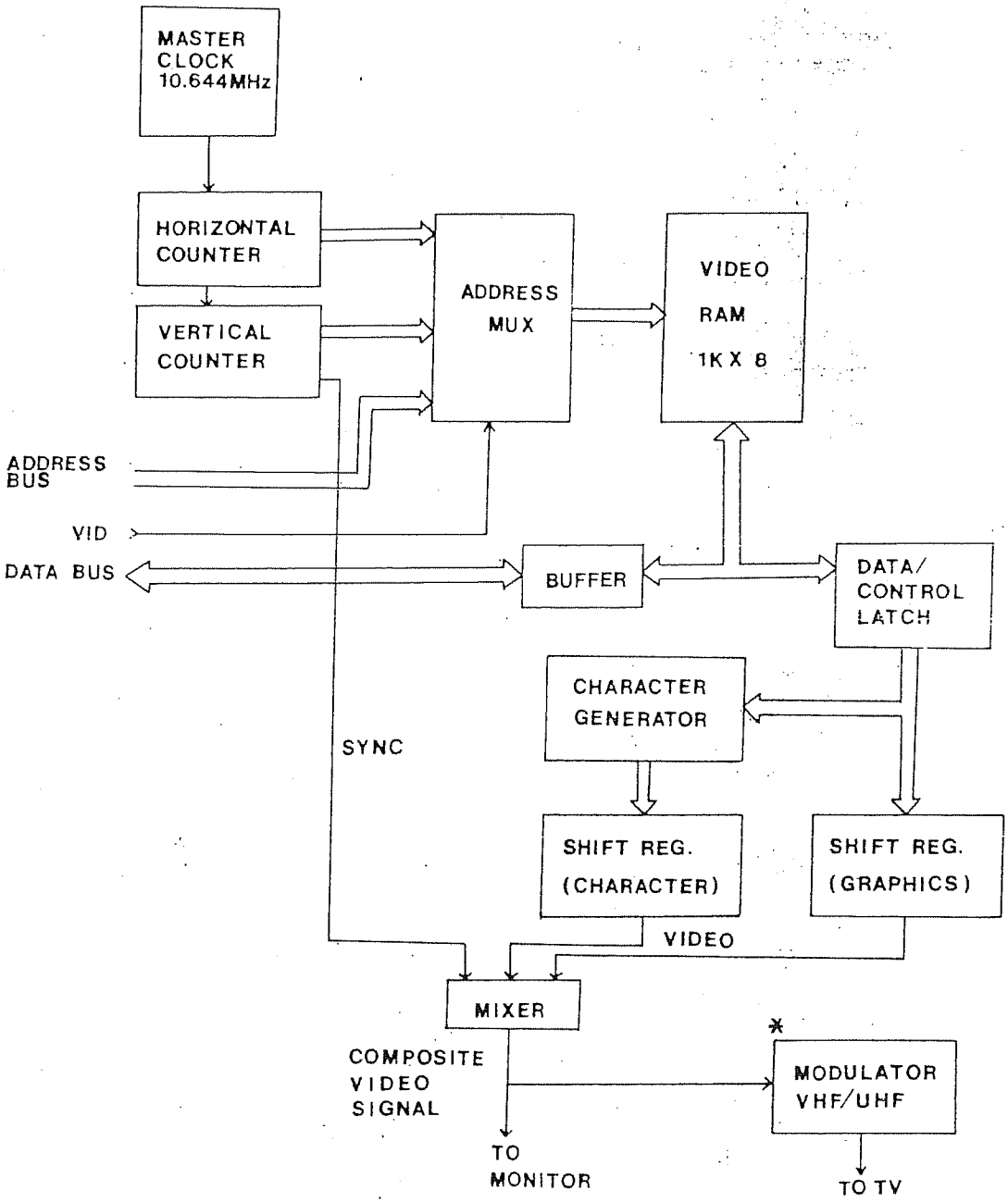
The memory cells of 4116 require periodic refresh within every 2 msec. During clock states T3 and T4 of an op-code fetch cycle, the CPU puts a memory refresh address on the address bus, and $\overline{MREQ}$ becomes active. Since $\overline{RAS}$ is the same as $\overline{MREQ}$, the RAM receives a row address, and that row of memory cells are refreshed. The refresh address is incremented by one in every op-code fetch cycle. The related timings are referred to the Z-80 data sheet in the appendix.

1.4 VIDEO INTERFACE

This section will reveal how the horizontal and vertical synchronization signals, and how the video signals are generated. In addition, we shall discuss how the video RAM's are accessed by the CPU, and are used to store the information displayed on a screen.

The structure of the video interface is illustrated in the block diagram of Fig. 1.4. It will be detailed in the following sub-sections.

Fig. 1.4 BLOCK DIAGRAM OF THE VIDEO INTERFACE



*NOTE: GENIE I ONLY.

1.4.1 Horizontal and Vertical Sync Signals

These two sync signals are generated by a divider chain with master clock of 10.644 MHz. The format of 64 characters/row x 16 rows is assumed in the following sections. Z36, Z35 and Z34 are the horizontal counters, and Z33 and Z32 are the vertical counters. The divider chain is shown in Fig. 1.5. Note that a character or a graphic unit is inside a 6 x 12 dot matrix.

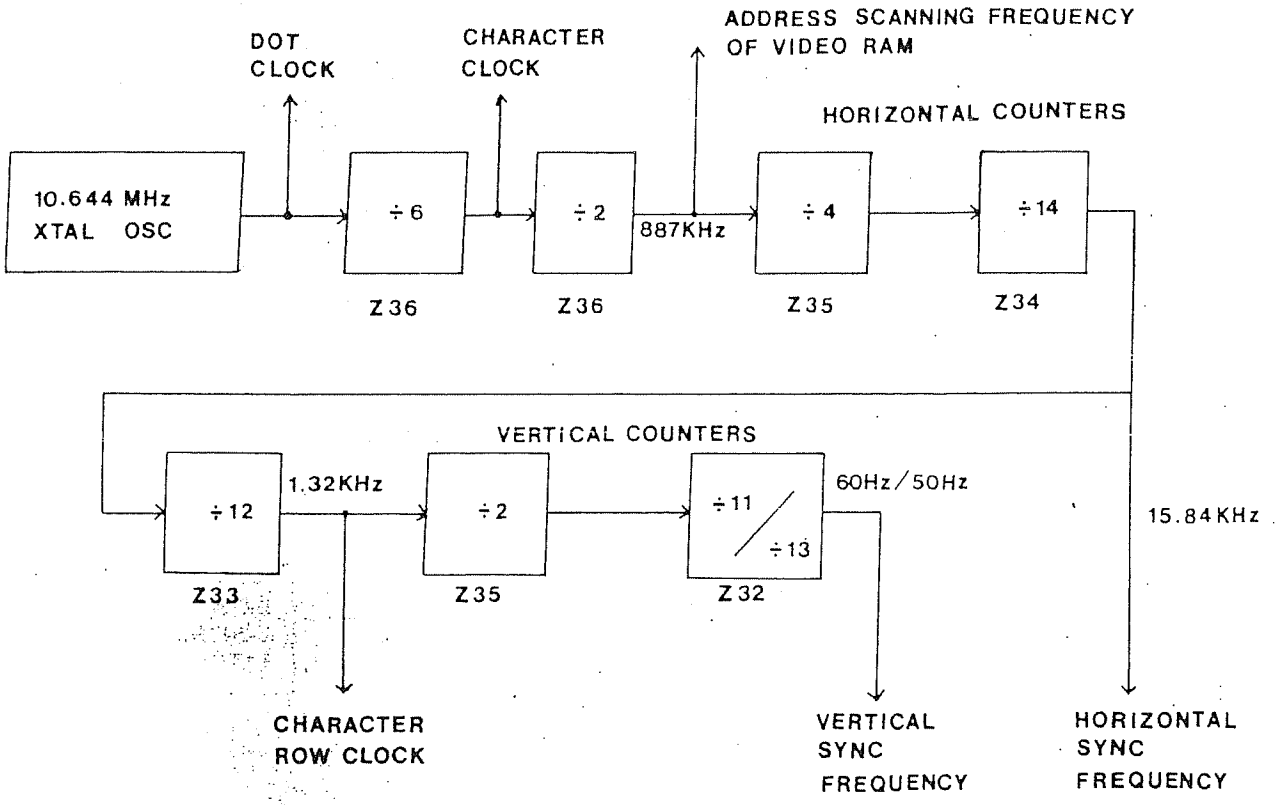
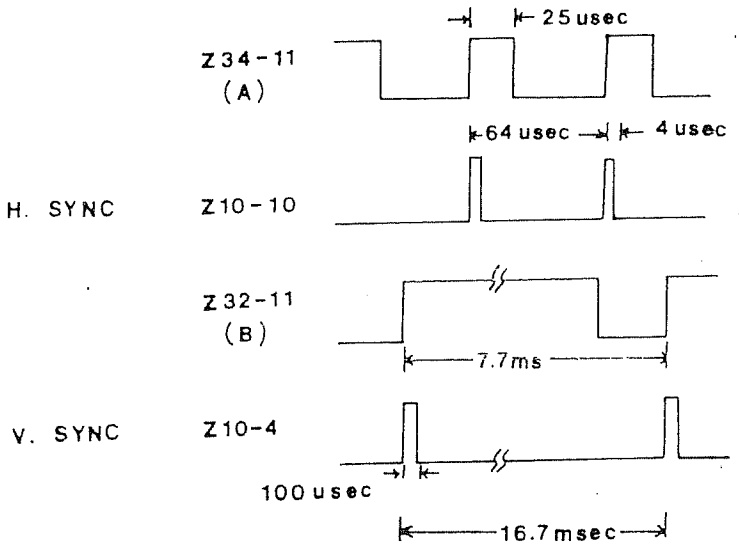


Fig. 1.5 DIVIDER CHAIN OF VIDEO DISPLAY

The outputs at Z34 — 11 and Z32 — 11 are the horizontal and the vertical sync frequencies (15.84 KHz and 50/60 Hz) respectively. These two sync frequencies will be shaped into the required sync pulses to a video display unit. First, VR1, C17 and four inverters (4069) delay the horizontal sync clock from Z34, while VR2, C16 and four inverters delay the vertical sync clock from Z32. Hence, we can shift the picture position by adjusting VR1 and VR2. Then, the two delayed signals are separately shaped into the desired sync pulses by a monostable circuit which contains a RC differentiating network and two inverters. The two sync pulses are shown in Fig. 1.6 Z22 forms an exclusive-OR gate, and sums up the horizontal and vertical sync pulses into the composite sync signal which is then fed to the video mixer to generate the composite video signal. (See section 1.4.3. on composite video signal).

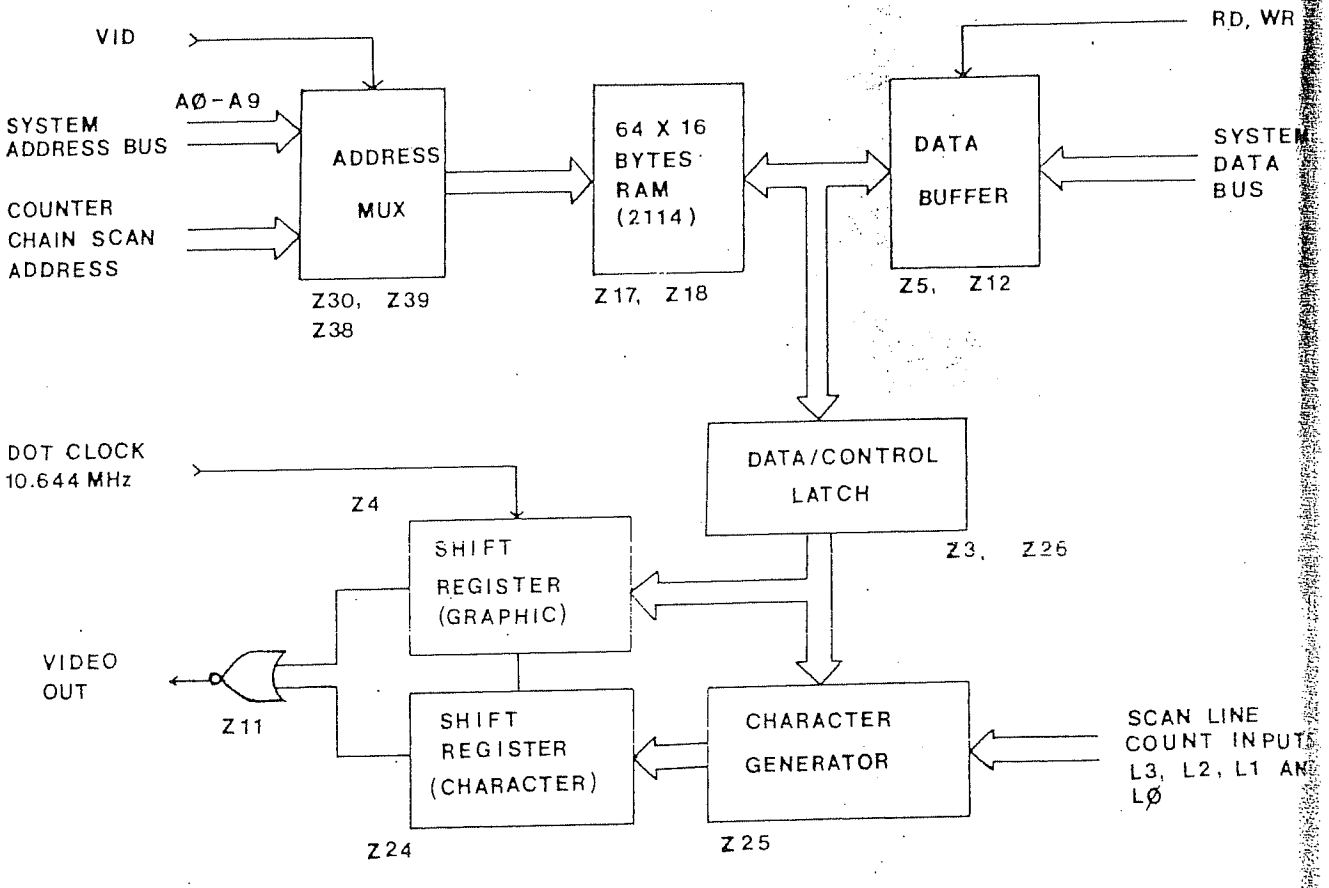
Fig. 1.6 **HORIZONTAL AND VERTICAL SYNC PULSES**



1.4.2 Video Memory

The video memory stores up the video information displayed on the screen. The memory is composed of two static RAM chips, 2114 each of 1K x 4 bits with access time less than 450 nsec. The circuit blocks interfacing with the RAM are illustrated in Fig. 1.7.

Fig. 1.7 VIDEO RAM INTERFACING



1.4.2.1 Video RAM Addressing

The video RAM are addressed by either the CPU or the counter chain. In order to display a character at a certain position on the screen, the CPU has to write the ASCII code of the character into the corresponding location of the video RAM. The video RAM has address bits, A0 – A9 in which A0 – A5 specify one of the 16 rows. The 64 x 16 characters are memory mapped onto the 64 x 16 locations of the video RAM.

As the CPU is going to access the video RAM (3CØØH – 3FFFH), the address decoded signal, VID from the CPU board will be LOW. The address multiplexers Z30, Z39 and Z38 switch to the system address bus. At the write mode, the $\overline{WR}$ signal will set the RAM's $\overline{W}$/R line LOW and enable the input buffers, and then the data on the data bus will be stored into the RAM. At the read mode, the $\overline{RD}$ signal enables the output buffers, and the RAM will put the addressed data onto the data bus. Notice that the display is blanked during the CPU's access to the video RAM because VID sets the data/control latch Z3 and Z26 to the CLEAR state through Z40-6.

It is required to maintain a continuous display of information on the screen so that the video RAM will be scanned periodically by the counter chain. 64 video memory locations are read in sequence during the scanning of each line. Each row of characters occupies 12 scanning lines, and therefore, the vertical address increases by one every 12 lines. The outputs of the counters are connected to the RAM's address inputs through multiplexers Z29, Z30, Z37, Z39 and Z38. They are listed as below:

Horizontal Count	RAM Address	Vertical Count	RAM Address
Z36-8	A0	Z32-14	A6
Z35-9	A1	Z32-12	A7
Z35-8	A2	Z32-9	A8
Z34-12	A3	Z32-8	A9
Z34-9	A4		
Z34-8	Z5		

1.4.2.2 Video Signal Generation

In alphanumeric mode, the character generator is the essential part in producing the video signals. The character generator is MM52116 FDW (or custom chip, E3004) which provides upper case and lower case characters in a 5 x 9 dot matrix. Recall that each row of characters is composed of 12 scanning lines. The line count signals L3, L2, L1 and L0 of the character generator come from pin 11, 8, 9 and 12 of Z33 respectively. Z33 is the divide-by 12 vertical counter.

D7 of a character data is zero whereas that of a graphic data is one. As the video RAM is addressed by the counter chain, Z17 and Z18 (2114) are set to the READ mode. The ASCII code of a character from the RAM's are latched into Z26 and Z3 at the rising edge of the strobe at Z28-3. See Fig. 1.8(a). The character generator, Z25 is addressed by the six data bits from the latches, Z26 and Z3. The character generator will output the corresponding 5-bit dot signals of the character on the scanning line defined by L3-L0. When Z36 counts to 5, Z28-3 will be LOW, and then Z2-6 will also be LOW. The outputs of the character generator will be loaded in parallel into the shift register Z24. When Z28-3 becomes HIGH again, the dot signals will be shifted out serially from Z24-13 at the rate of the dot clock 10.644 MHz. Meanwhile, during the rising edge of the strobe at Z28-3, the next character will be latched into Z26 and Z3, ready for being shifted out next.

Fig. 1.8(a) VIDEO DISPLAY TIMING OF A CHARACTER

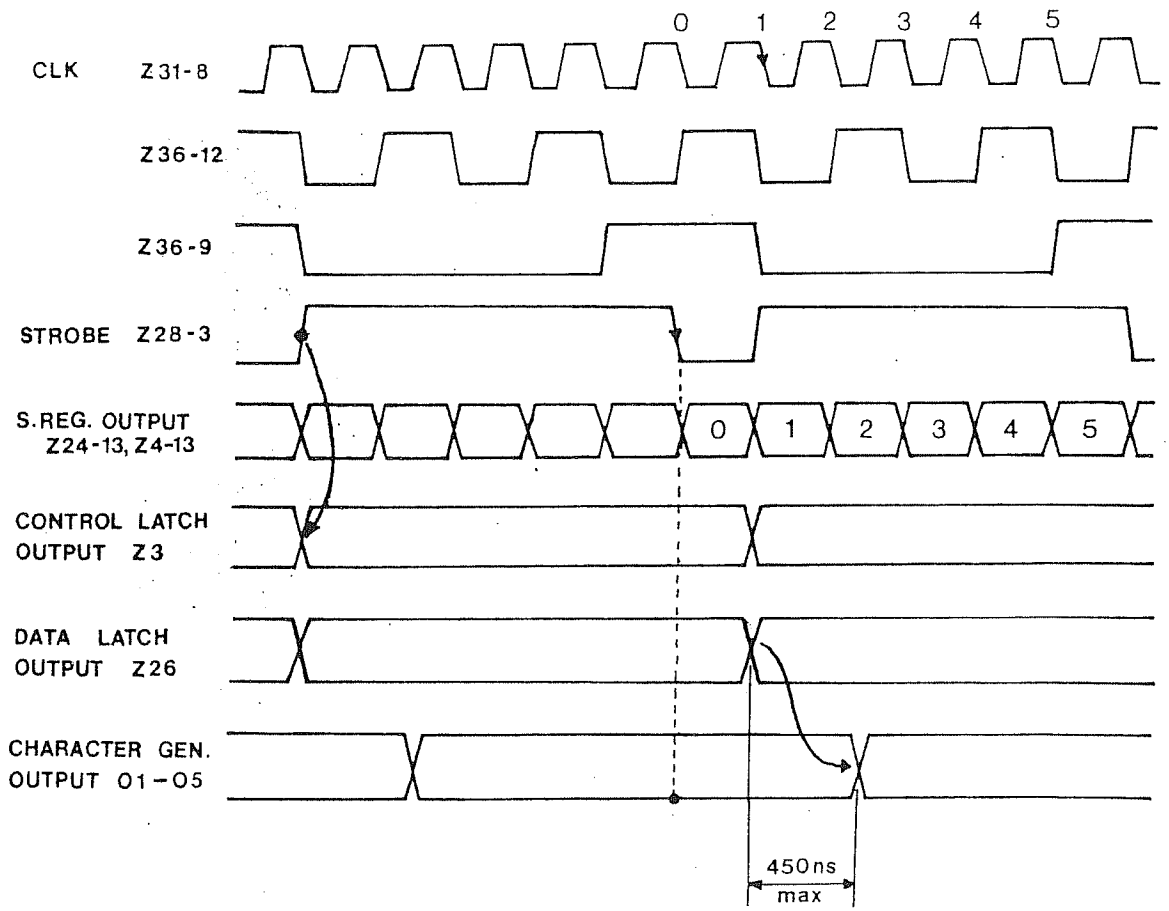
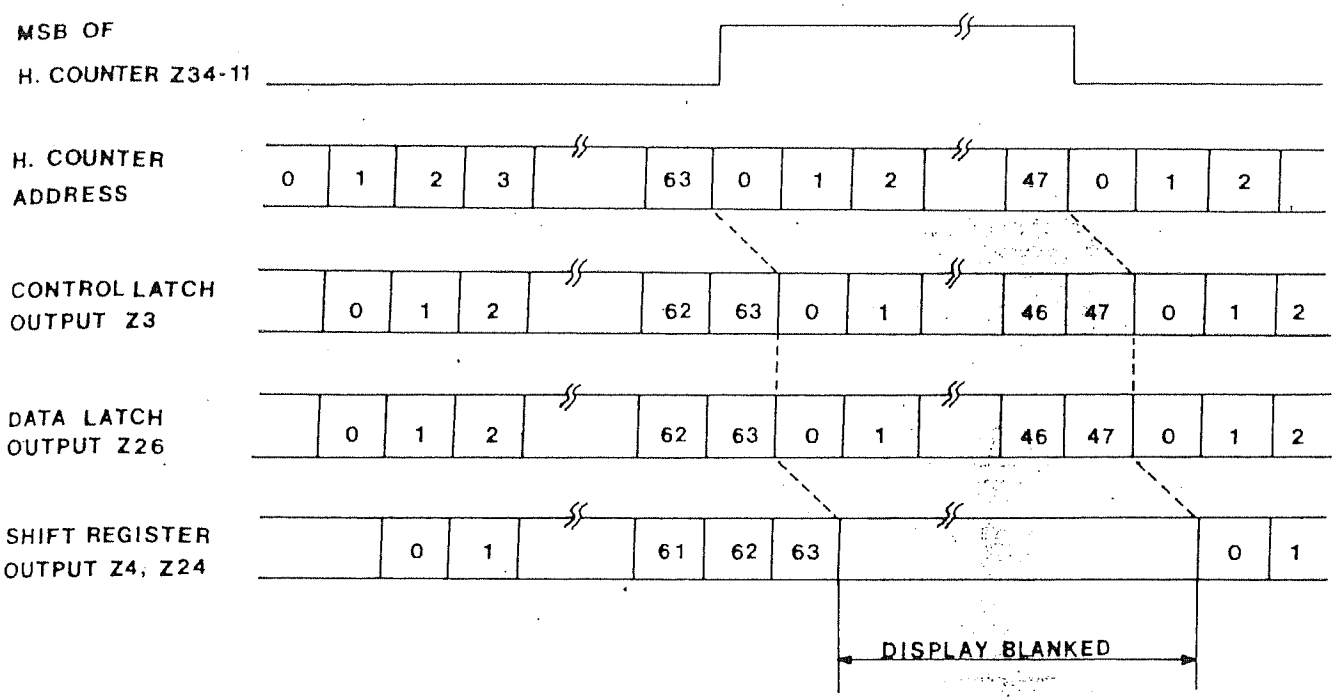


Fig. 1.8(b) VIDEO DISPLAY TIMING OF A LINE



NOTE: The numbers in the control and data latch timings represent the control or data signals of the corresponding horizontal address.

In the graphic mode, each row contains 64 graphic units in 12 scanning lines, and each unit is made up by 6 cells. Each cell corresponds to one data bit in the RAM. Details refer to section 1.4.4.2 on graphic data.

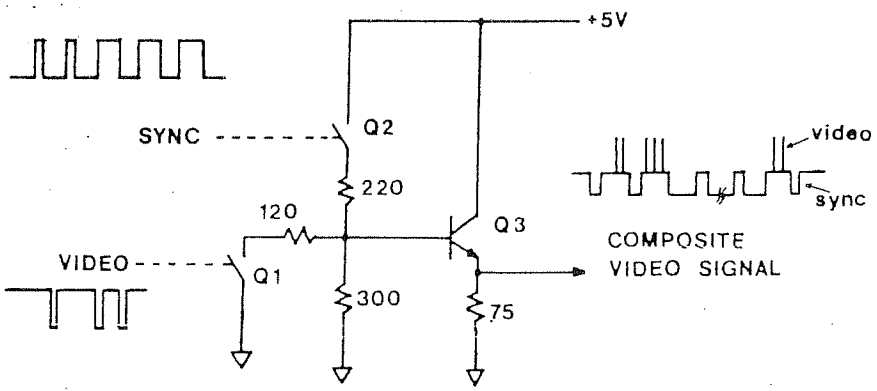
The generation of video signals in the graphic mode is similar to that in the character mode. They differ in that a multiplexer, Z27 and shift register, Z4 are used in the graphic mode. Since D7 of a graphic data is one, and then Z3-7 is HIGH, Z4 will be enabled to accept the graphic data from Z27. The dot signals will be shifted out serially at Z4-13 at the rate of 10.644 MHz. Note that the multiplexer, Z27 is controlled by L3 and L2, and the graphic data from the latch, Z26 are fed to Z27 instead of the character generator, Z25.

Display blanking is achieved as follows. Scanning lines 9-11 in the character mode are automatically blanked because the outputs of the character generator will be zero during these 3 lines. The horizontal and vertical blanking signal comes from Z11-1 and inhibits Z24 and Z4 from getting parallel data from Z25 and Z27 respectively. The display is blanked during the period of screen boundary and retrace when the horizontal or vertical sync signal is HIGH at pin 2 or 3 of Z11 respectively. See Fig. 1.8(b).

1.4.3 Composite Video Signal

The horizontal sync and the vertical sync signals are combined by Z22, and this composite sync signal is fed to the base of Q2. Q1 and Q2 act as two switches. Q3 forms a mixing circuit, and the sync and video signals are summed up at the base of Q3. Fig. 1.9 shows the simplified composite video mixer. The composite video signal so formed will be sent to the video monitor or the input of a built-in VHF or UHF modulator. Note that GENIE II does not have a modulator and cannot use a TV as the video display without modifications.

Fig. 1.9 EQUIVALENT CIRCUIT OF VIDEO MIXER



1.4.4 Display Modes

The GENIE has two display modes, namely, character mode and graphic mode. Data bit 7 of the video memory determines the mode of display; character mode is selected when D7 is logical '0' and graphic mode when D7 is logical '1'.

1.4.4.1 Character Mode

The characters displayed are in alphanumeric format, and their ASCII codes are stored in the video RAM's. In the preceding sections, 64 characters/line mode is assumed. GENIE I system has a push-button, S1 at the back panel of the unit to select either 64 characters/line or 32 characters/line mode. GENIE II system has no 32 characters/line mode of display.

In 32 characters/line mode, switch S1 is closed. Multiplexers Z29 and Z37 are switched to the other four inputs. The reference counter clock becomes CLOCK/2 so that the horizontal/vertical counting frequencies will be scaled down by two. The PAGE switch chooses the left page when LOW, and chooses the right page when HIGH. This is obvious because A5 of the video RAM is connected to the PAGE signal through the multiplexer Z37, and address bits A0 — A5 select one of the 64 columns in the 64 x 16 units of bytes of video memory.

1.4.4.2 Graphic Mode

D7 is logical one when graphics are to be displayed. The shift register Z4 is enabled. The graphic data from the video RAM are latched into Z26, and the outputs of Z26 are multiplexed by Z27 (74LS153) selecting two out of six bits each time. The selection is controlled by the line count signals, L2 and L3. A graphic cell is specified as below.

1 graphic unit

(6 graphic cells)

DØ	D1
D2	D3
D4	D5

D0 and D1are selected for scan lines 00 – 03, D2 and D3 for scan lines 04 – 07, D4 and D5 for scan lines 08 – 011.

The display formats of the character/graphic modes are shown in Fig. 1-10.

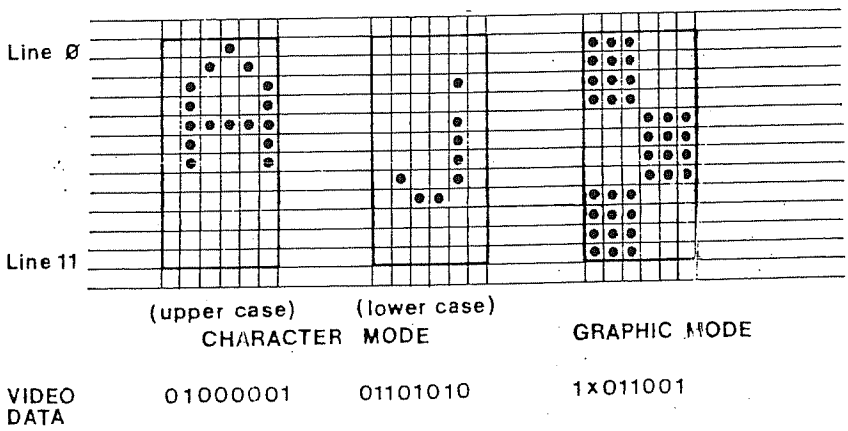
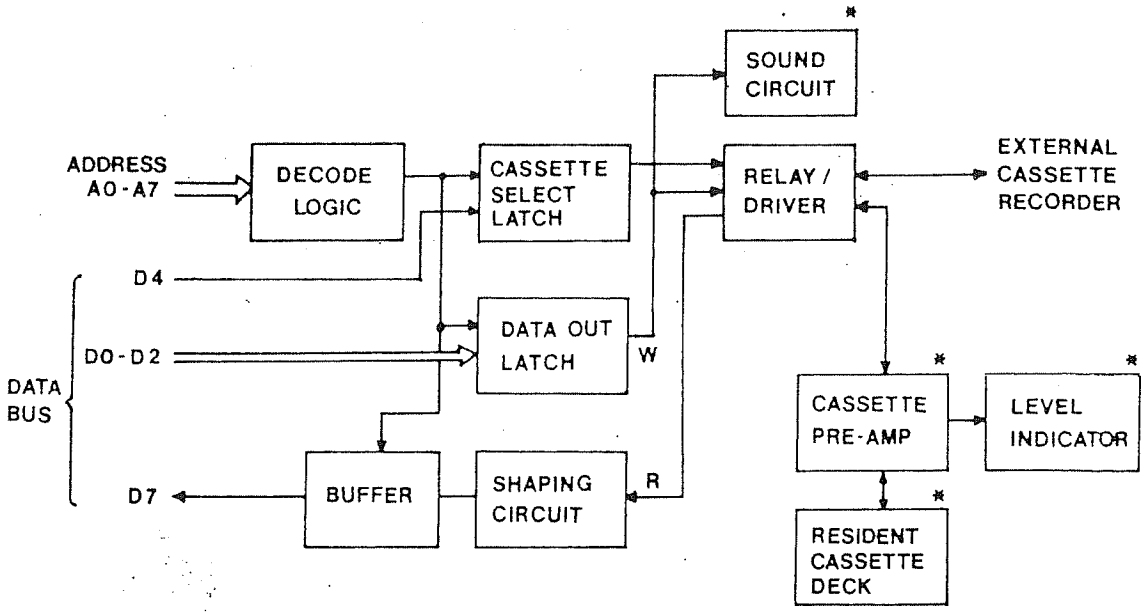


Fig. 1-10 CHARACTER/GRAPHIC DISPLAY FORMAT

1.5 CASSETTE INTERFACE

The cassette interface consists of the following parts: address decoding, latches, cassette select and relay drivers, rectifying and shaping circuit, and cassette preamplifiers and output level indicator. See Fig. 1.11. Sound effect circuit also uses the cassette output port.

Fig. 1.11 CASSETTE INTERFACE



*NOTE : These parts are absent in GENIE II.

1.5.1 Addressing/Decode

Z19, Z31 and Z20 generate the address decode signals and the I/O control signals. Table 1.1 shows the I/O port assignments.

Table 1.1 CASSETTE I/O PORT

PORT	DATA BITS			HIGH	LOW
Output, FF	D2			Cassette ON	Cassette OFF
	D0, D1	signal	output		
Input, FF	D7	signal	input		
Output, FE	D4			Cassette 2 Selected (external)	Cassette 1 Selected

1.5.2 Cassette Selection

The CPU selects either cassette 1 or cassette 2 through the output port FE with data line, D4. The selecting signal from D4 is latched by Z40, and outputs at Z40-8 ($\overline{Q}$) and Z40-9 (Q). cassette 1 is selected as D4 is LOW, and Q7 and Q8 will turn ON provided D2 (at Z6-2) is HIGH. Relay REL1 will be activated, and the READ, WRITE and motor drive lines of the resident cassette 1 will be connected to the cassette interface.

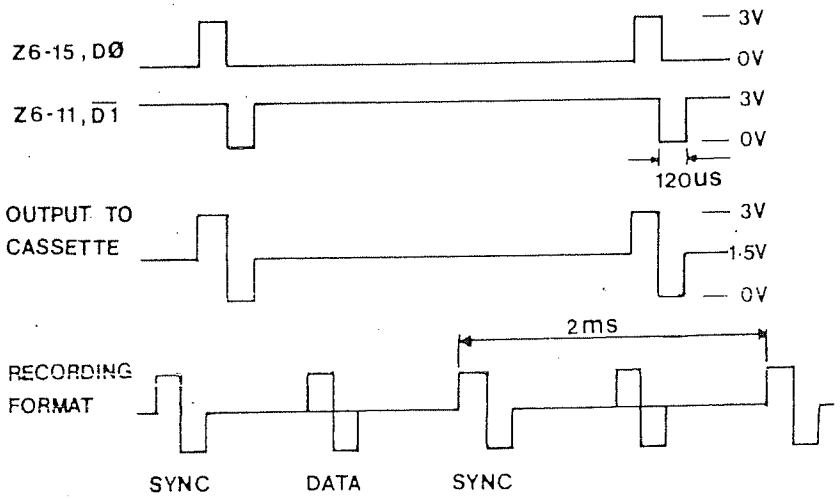
As D4 and then Z40-9 are HIGH, Q5 and Q6 will turn ON if D2 at Z6-2 is also HIGH. Relay REL2 will be activated, and the cassette input, output and remote control lines of an external cassette recorder will be properly connected to the cassette interface through a 5-pin DIN socket K3.

GENIE II system can only operate with an external cassette recorder so that the circuitry for the resident cassette is omitted. Compare the schematics of cassette interface of GENIE I and II.

1.5.3 Cassette Write

The idealized recording signal to be stored on the cassette tape is shown in Fig. 1.12. This signal is formed by data D1, D0 and a summing circuit at Z6-11 ($\overline{Q}$) and Z6-15 (Q). The logical outputs of D1 and D0 are software controlled to construct the desired recording signals.

Fig. 1.12 CASSETTE WRITE SIGNALS

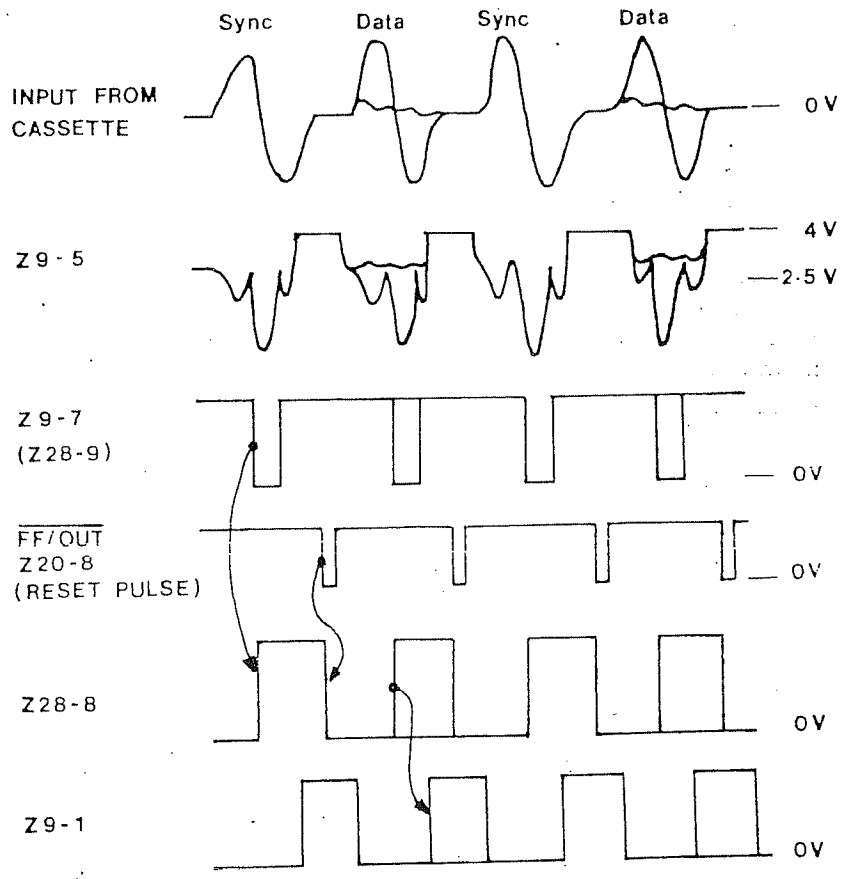


The data format stored on the cassette tape is as follows. At the beginning of cassette write (CSAVE), the CPU outputs 128 ZERO data bits, followed by a code A5H. The CPU will detect this code during cassette read (CLOAD) for synchronization. Next come a two-byte starting address and a two-byte ending address of the program in the RAM's. After all data have been written, a byte of check-sum is added for detecting errors during cassette read/write.

1.5.4 Cassette Read

Before the CPU can recognise the information retrieved from a cassette tape, the audio signal from the cassette recorder must be shaped into logical sync and data signals. The CPU and cassette routine will then convert the serial data into source programs which will be stored into the RAM's. The filtering pre-amplifiers formed by Z1 (LM324) on the cassette board amplify the small signals from the Read/write head. The amplified signal is buffered (Q1) and rectified to drive a level meter. This signal level indication is useful in cassette reading various tapes. We may obtain the proper signal level by adjusting the gain of Z1 (VR3).

Fig. 1.13 CASSETTE READ SIGNALS

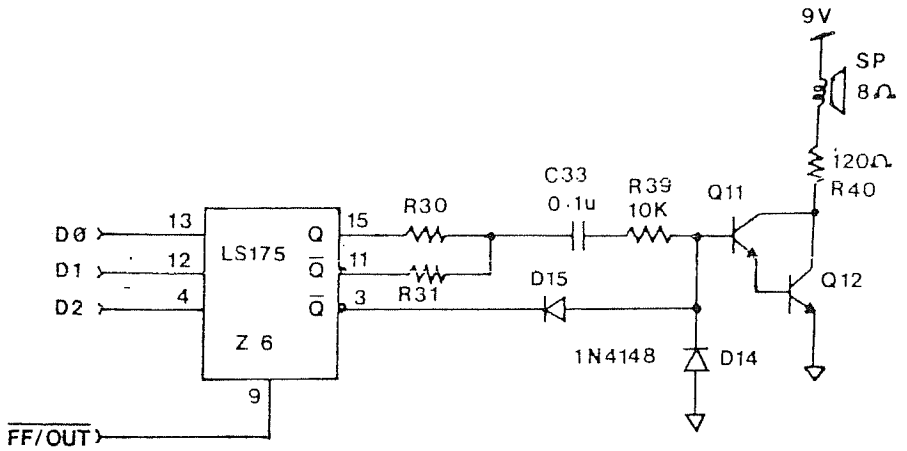


Z9 (LM324) on the interface board converts the audio signal from the recorder into serial digital signal. The input signal is high-pass filtered, and then full-wave rectified. Negative-going pulses are obtained at Z9-7, the output of a level detector. Z9-7 is connected to Z28-9. Z28 forms a R-S bistable latch, and Z28-8 is connected to the data line, D7 through a buffer, Z7. Z28-8 is triggered to HIGH by the falling edge at Z9-7. As soon as the CPU has read a logical 1 at data line D7, it will reset the bistable latch after 500 usec. Upon detecting the leading zeroes and the sync code (A5H), the CPU should be synchronized with the serial data stream. It will strobe the data pulse at 1 msec after the sync pulse and reset the bistable latch. Pulses at Z28-8 are delayed for about 250 usec and output at Z9-1. The delayed pulse pulls up the signal at Z9-5, and therefore, the signal-to-noise ratio is increased.

1.5.5 Sound Output (GENIE I only)

Apart from video display, sound effects are another way of communication between a man and the Genie I microcomputer. This is implemented simply by an audio driver (Q11 and Q12 darlington) and a built-in loudspeaker. The sound circuit is connected to the cassette output port FFH. The sound output is determined by the software outputting various data stream to D0 and D1 of the output port. See Fig. 1.14. The sound stops during CSAVE because the base of Q11 is pulled LOW by Z6-3 ($\overline{Q}$ of D2). D2 of the output port FFH becomes HIGH during cassette ON.

Fig. 1.14 SOUND CIRCUIT (ON INTERFACE BOARD)



1.6 KEYBOARD

Keyboard is the only device we can input commands to the GENIE. The key matrix is memory mapped with addresses from 3800H to 3880H, and locations 3800H – 3BFFH are reserved for keyboard use. Refer to the memory map in Fig. 1.2.

There are two locked switches, F1 and PAGE which are not included in the key matrix. They directly control the hardware of the resident cassette recorder and the display modes respectively. These two keys are absent in GENIE II which has no resident cassette recorder.

1.6.1 Key Matrix

The key matrix is formed by 8 inverted address lines AKØ – AK7 and 8 inverted data lines DKØ – DK7. The matrix is illustrated in Fig. 1.15.

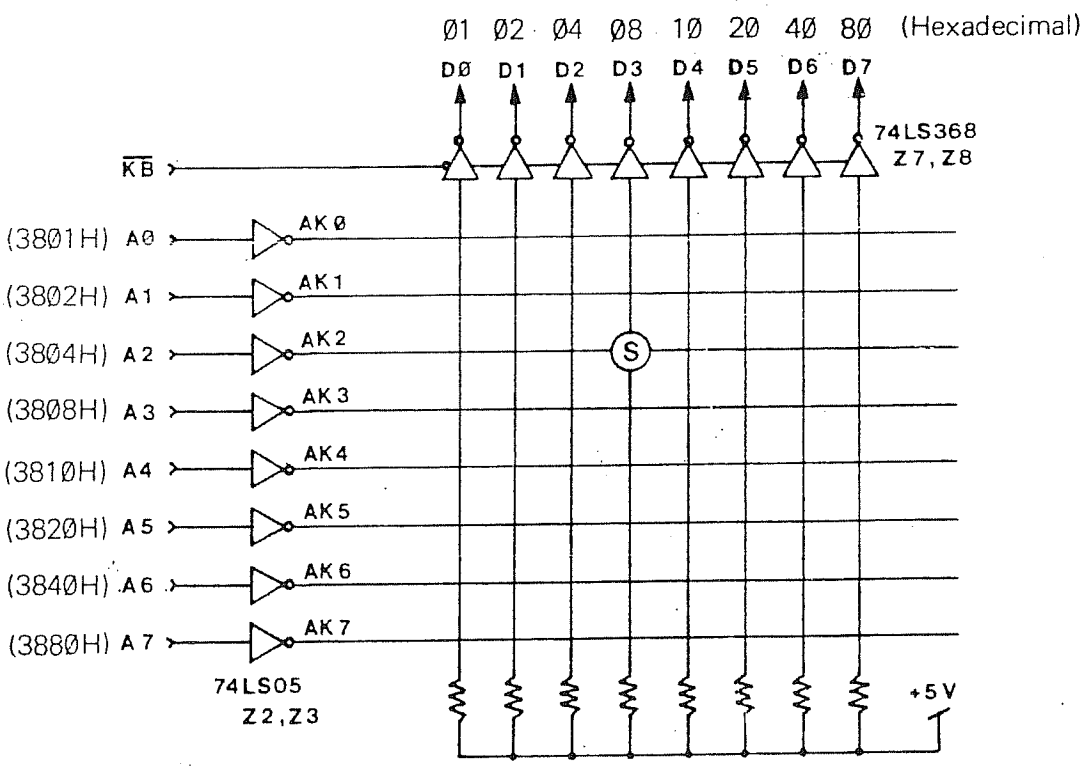


Fig. 1.15 KEY MATRIX

The inverting buffers, Z7 and Z8 are controlled by the keyboard strobe, $\overline{KB}$ which is derived from Z35 – 11 on the CPU board. Refer to section 1.1.4. $\overline{KB}$ is active LOW when the CPU is accessing the memory locations 3800H – 3BFFH. AKØ – AK7 are the open-collector outputs of Z2 and Z3 (74LS05).

While no key is pressed, DKØ – DK7 are all HIGH since they are pulled up to +5V by resistors. The CPU reads ØØH, indicating no key is pressed. The keyboard routine in the system ROM scans through the AØ – A7 lines repeatedly, making one address line logic HIGH each time. See Fig. 1.15. When any key is depressed, the CPU will detect a logic HIGH on the corresponding data line as soon as the corresponding address line is scanned. For instance, key S is depressed. The DK3 line will be connected to the AK2 line, and DK3 will be LOW as A2 is logic HIGH. Then, the CPU will read Ø8H into the accumulator from the memory location 3804H. The keyboard routine will decode it into the ASCII equivalent of the character S. Except the command keys, the ASCII codes of the characters or symbols keyed in will be written into the video RAM and displayed.

1.6.2 Numeric Keypad (GENIE II only)

This keypad contains the numeric keys and 4 function keys. The numeric keys have the same positions on the key matrix as the main keyboard. The function keys are user programmable and occupy the AK3 line of address 3808H. Refer to the schematic of the keyboard.

1.7 POWER SUPPLY

The power supply unit which is in a heat-resisting plastic box delivers full-wave rectified +8VDC, +16VDC and −16VDC. The two power transformers have secondary voltages of 9.6V x 2 and 15V x 2 respectively. At the primary side of the transformers, there is a line filter network composed of a parallel ceramic capacitor of 0.01uF and two series RF chokces. Overvoltage protection is provided by a varistor across the ac mains. The metal oxide varistor has a breakdown voltage of 275V with 55 joules. Over-load and short-circuit damages are minimized by a fuse of 1A (117V) or 0.5A (220V/240V) in series with the ac mains.

The specifications for the output voltages of the power supply unit are as below.

Voltage	No load voltage		Full load voltage		Remark
	Min.	max.	min.	max.	
+8V	10.5V	11.5V	8V	9V	FL +8V @ 1.2A
+16V	20V	24V	15V	18V	FL +16V @150mA
−16V	20V	24V	15V	18V	FL −16V @ 100mA

Linear IC regulators 7805 and 7812 on the CPU board supply +5V and +12V respectively. A simple zener regulator provides −5V for the dynamic RAM's. On the interface board, +9V supply is obtained from +16V by a transistor/zener regulating circuit (Q10 and 8.2V zener diode). +9VDC is required for driving the relays on the interface board, the pre-amplifier (Z1, LM324) on the cassette board, and the motor of the resident cassette recorder.

2. TROUBLESHOOTING

2.1 INTRODUCTION

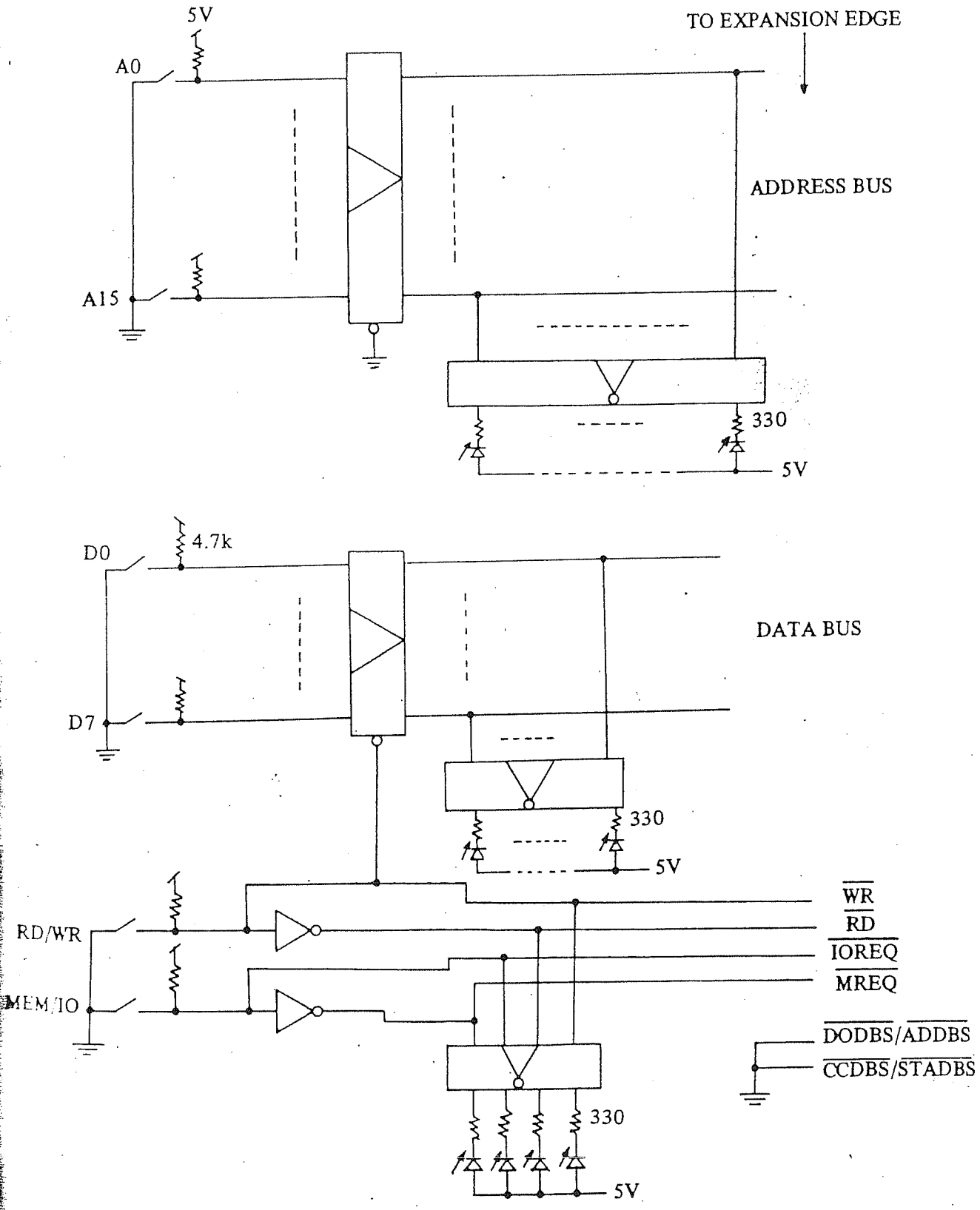
Three common types of fault are component failure, open circuit and short circuit. Since the GENIE has to pass a very strict quality checking, short circuit seldom occurs. Open circuit and failure of component are more common.

It may be caused by shock during transportation or running the GENIE under adverse conditions (eg. high temperature and high humidity).

2.2 BUS CHECK – DATA, ADDRESS AND CONTROL BUSES

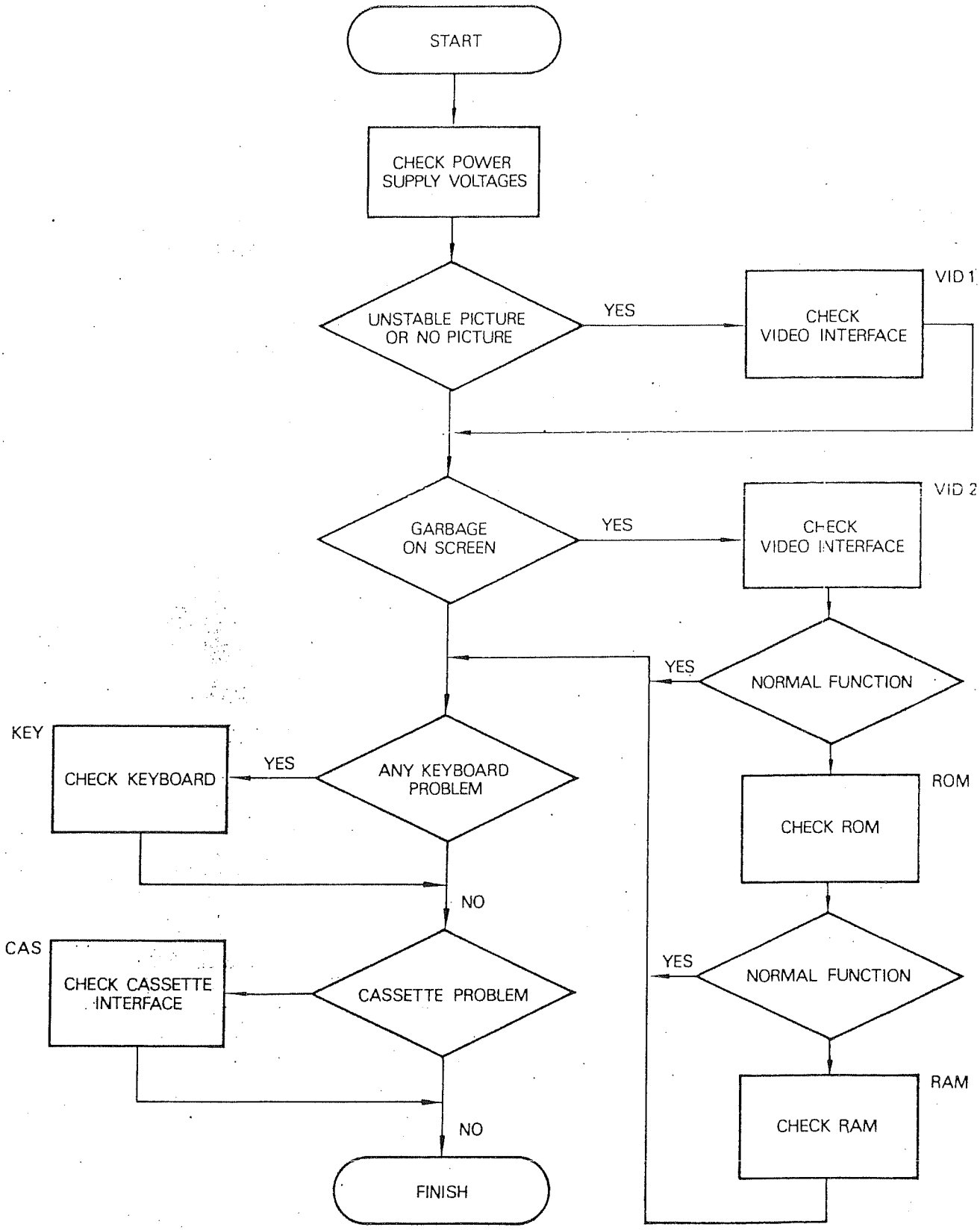
Bus check can be facilitated by a simple tester. It disables the CPU buffers and puts data, address and control signals on the buses. Therefore, short circuits and open circuits can be tested under static condition.

Fig. 2.1 TESTER CIRCUIT DIAGRAM



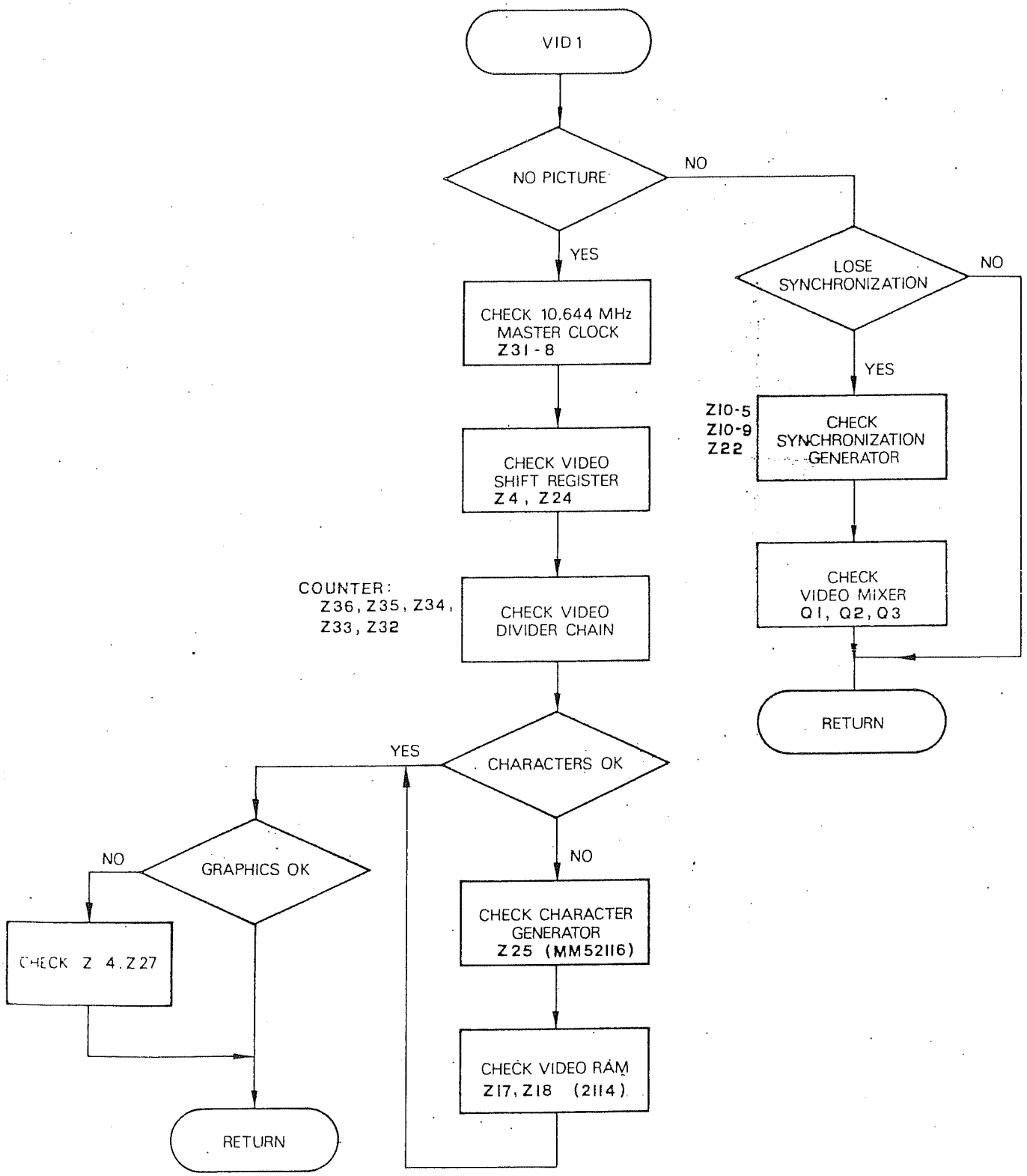
2.3 TROUBLESHOOTING FLOWCHARTS

General Flowchart in Troubleshooting

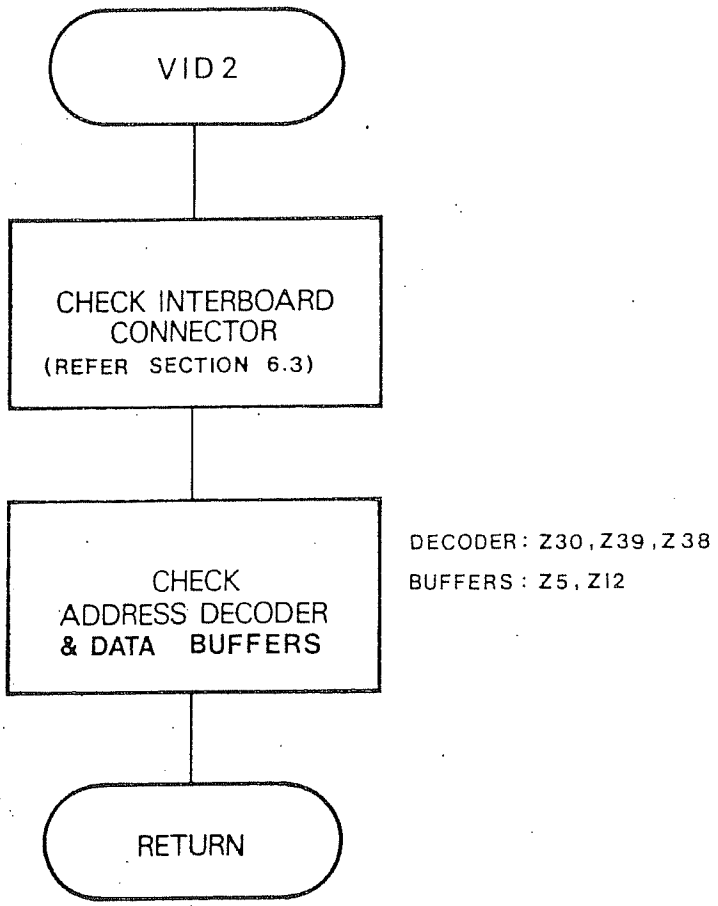


2.3.1 Video Interface

(Interface Board)



(Interface Board)

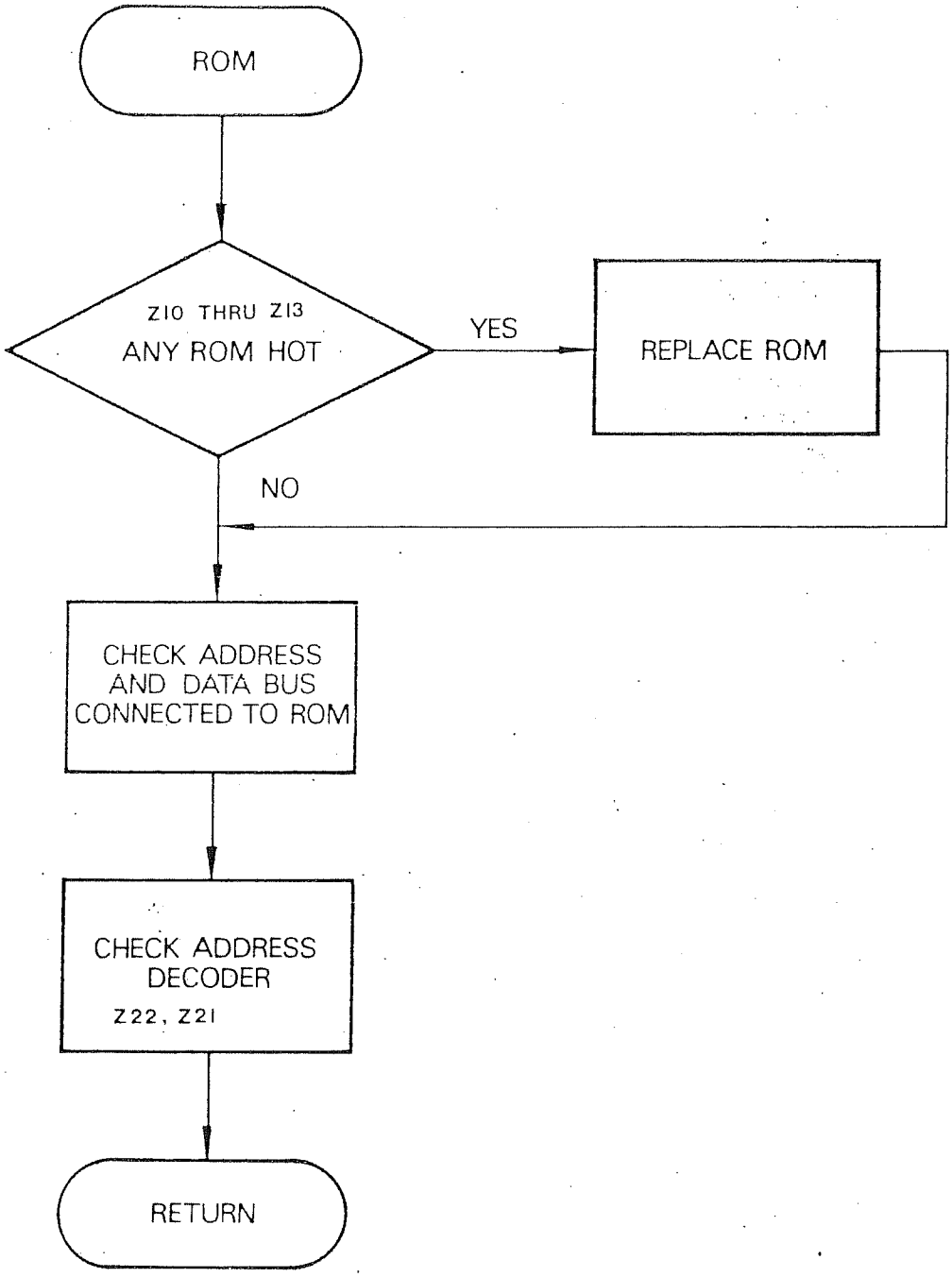


Remarks:-

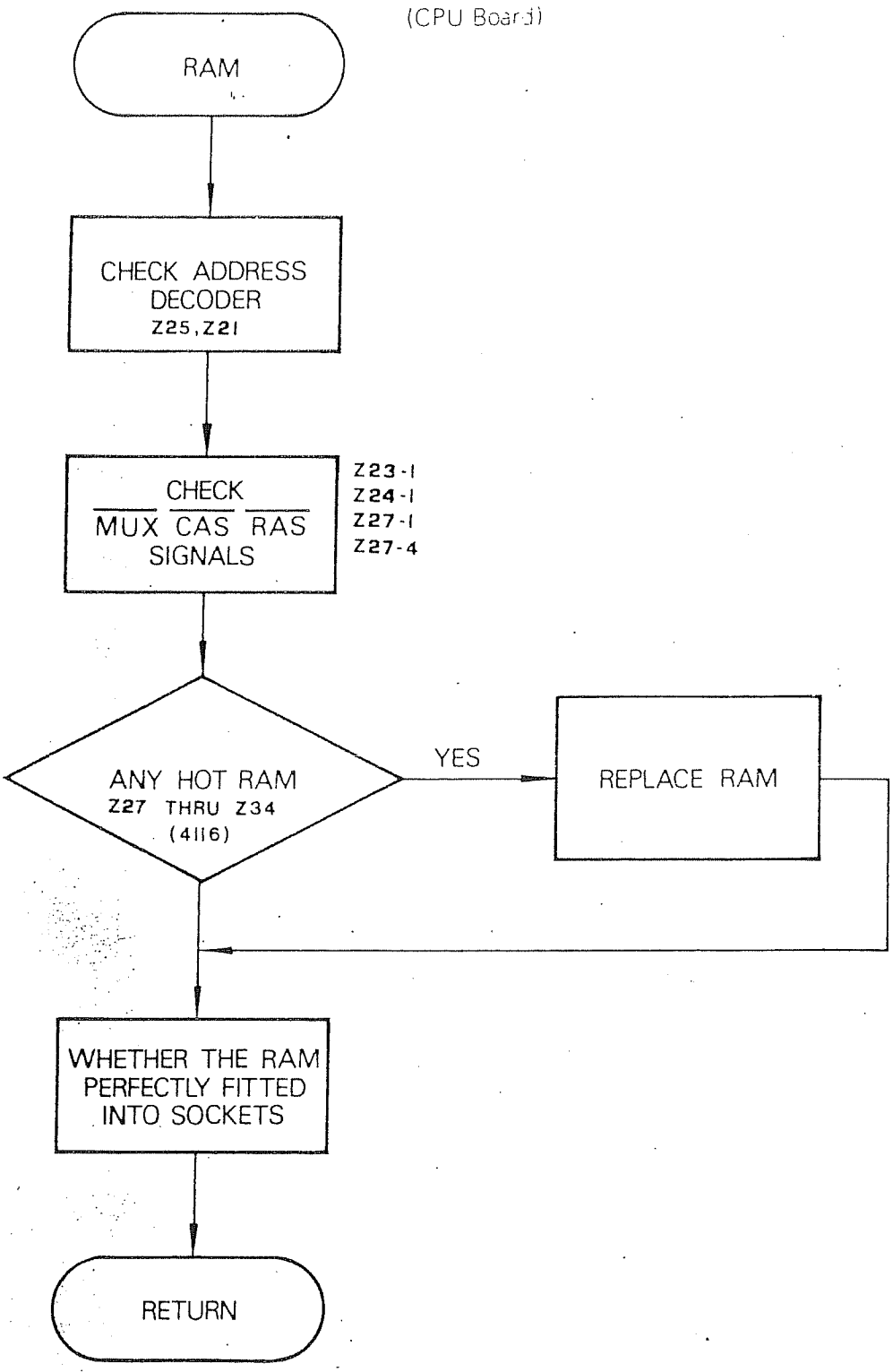
1) A system that mis-spells words usually has data screw-ups in the video RAM, or the data input to the character generator is being grabbed by a defect around latch Z26.
2) If the display oscillates up and down, it may be due to low supply voltage. See whether there is any ripple at the +5V supply.

2.3.2 System ROM's

(CPU Board)



2.3.3 User RAM

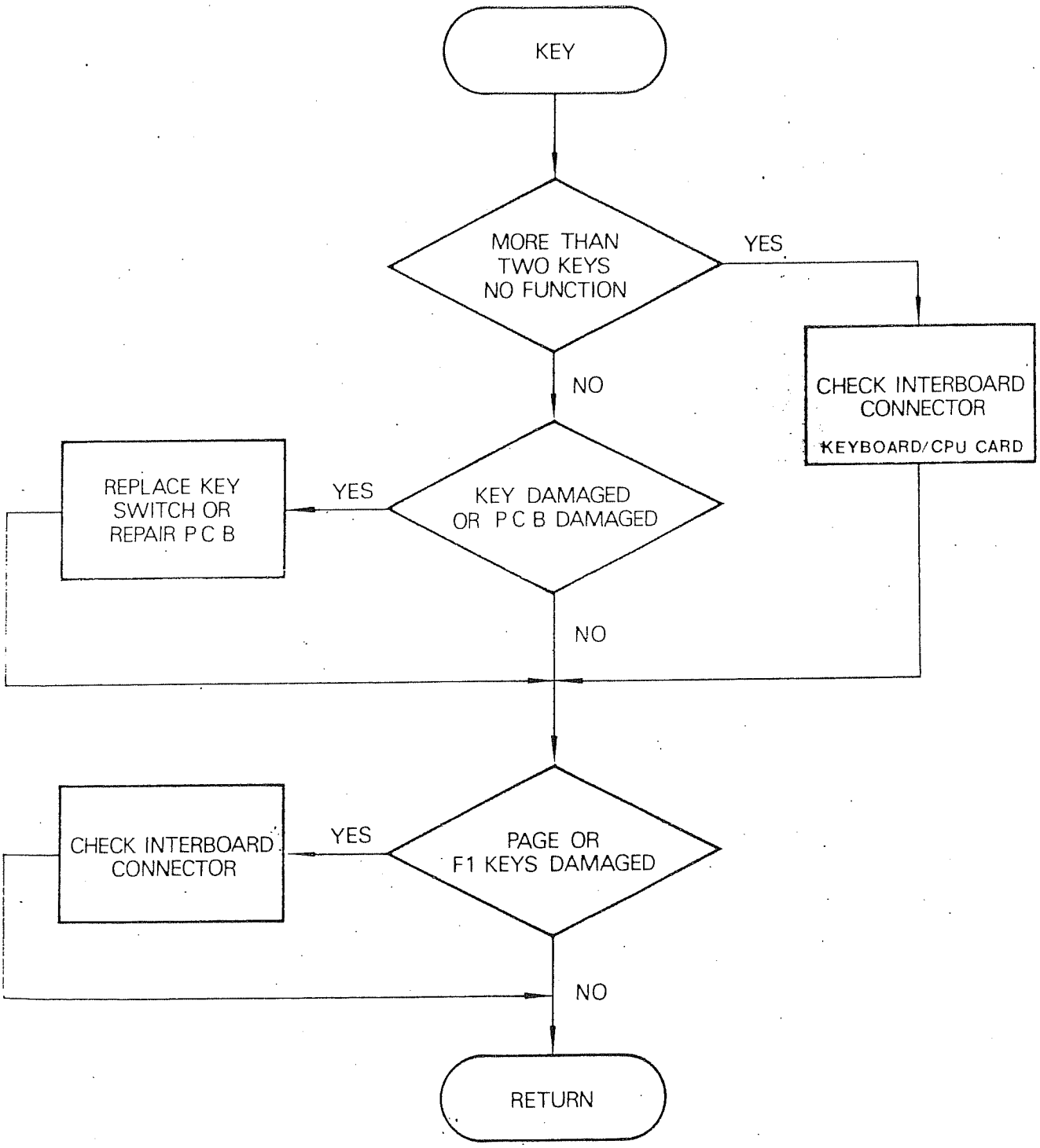


Remark:-

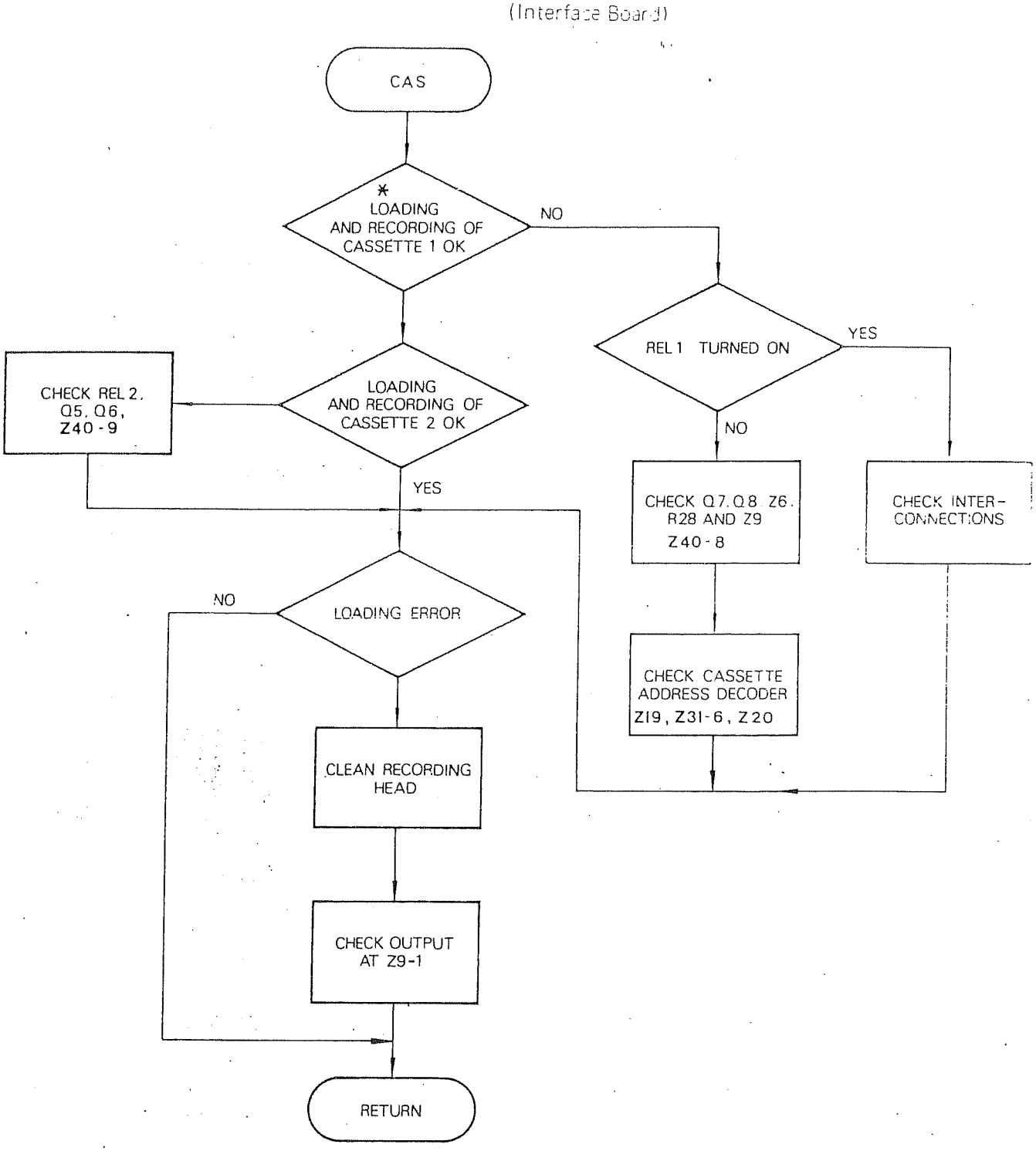
The flowcharts of RAM and ROM checking seems quite simple, but actually it is most difficult to determine whether the component is damaged. It is because the GENIE cannot work properly or fails intermittently. The best way to check these sections is to replace the RAM or ROM chips with good ones if other sections of the circuits are working normally.

Precaution: CPU, ROM and RAM chips should be placed on conductive materials after taking out from the circuit.

2.3.4 Keyboard



2.3.5 Cassette Interface



* skip this step for GENIE II system.

Remark: Sometimes, cassette loading error may not be caused by circuit fault, but due to the poor quality of the cassette tape.

3. PICTURE POSITION ADJUSTMENT

After the video interface has been serviced, the picture position should be adjusted so as to make the picture balanced in the centre of the screen.

Enter and run the following simple program. A rectangle showing the screen boundary will then be drawn. VR1 and VR2 should be adjusted with a non-metallic screw driver.

```
10   CLS
20   FOR X = 0 TO 127
30   SET (X, 0): SET (X, 47)
40   NEXT X
50   FOR Y = 0 TO 47
60   SET (0, Y): SET (63, Y): SET (64, Y): SET (127, Y)
70   NEXT Y
75   PRINT @ 522, "L E F T";: PRINT @ 554, "R I G H T",
80   GOTO 20
90   END
```

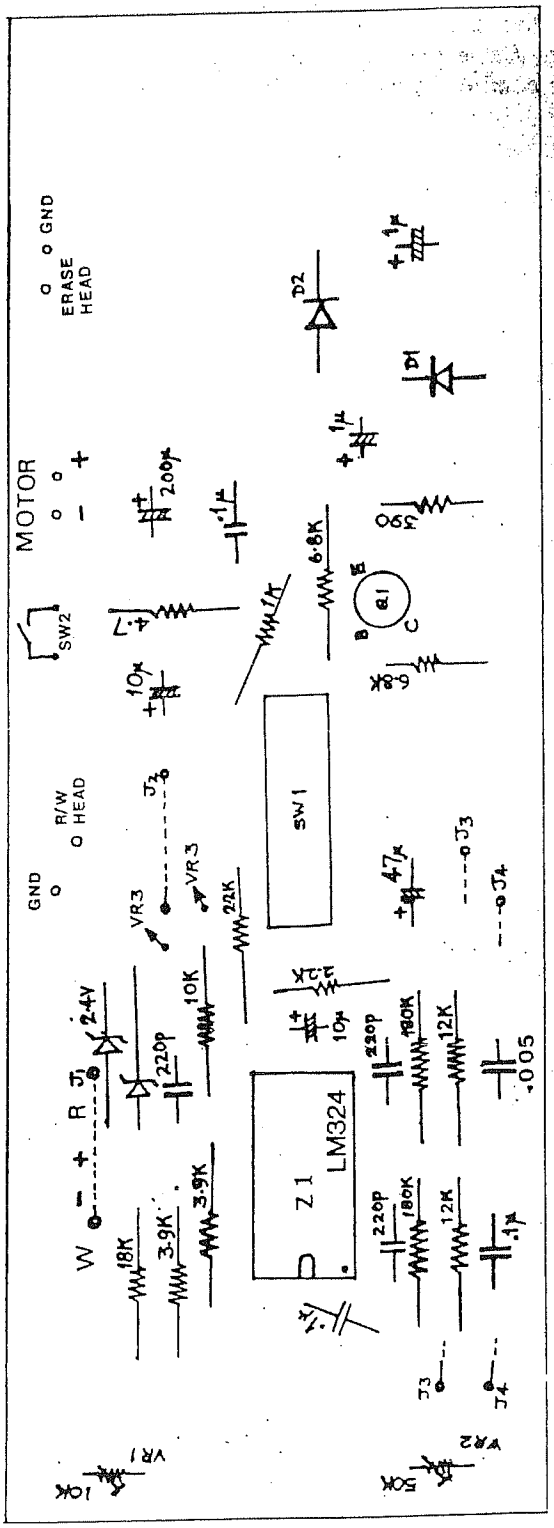
4. SCHEMATIC DIAGRAMS

5. COMPONENT LAYOUT DIAGRAMS

5.3 CASSETTE BOARD

(GENIE I ONLY)

EG3003 COMPONENT LAYOUT

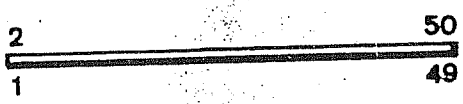


6. PIN ASSIGNMENTS OF CONNECTORS

6.1 EXPANSION INTERFACE BUS

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	A7	4	A6
5	A5	6	A4
7	A1	8	A3
9	A2	10	A0
11	D5	12	D2
13	NC	14	D1
15	D0	16	D3
17	D7	18	D6
19	VCC	20	D4
21	A15	22	A8
23	A14	24	A9
25	NC	26	A10
27	A13	28	A11
29	A12	30	PHI
31	$\overline{\text{PINT}}$	32	NC
33	NC	34	$\overline{\text{PHLDA}}$
35	$\overline{\text{PHANTOM}}$	36	$\overline{\text{HALT}}$
37	$\overline{\text{PWAIT}}$	38	$\overline{\text{IORQ}}$
39	$\overline{\text{PHOLD}}$	40	$\overline{\text{WR}}$
41	$\overline{\text{RD}}$	42	$\overline{\text{CCDBS}}/\overline{\text{STADBS}}$
43	$\overline{\text{MREQ}}$	44	$\overline{\text{DODBS}}/\overline{\text{ADDBS}}$
45	$\overline{\text{M1}}$	46	$\overline{\text{RESET}}$
47	$\overline{\text{RFSH}}$	48	$\overline{\text{NMI}}$
49	GND	50	GND

EXPANSION PIN EDGE
VIEWED FROM REAR SIDE



SIGNAL DESCRIPTION

PHI	1.78 MHz Clock
$\overline{\text{PINT}}$	Interrupt
NC	No Connection
$\overline{\text{PHLDA}}$	Processor Hold Acknowledge
$\overline{\text{PHANTOM}}$	Phantom
$\overline{\text{HALT}}$	Halt Acknowledge
$\overline{\text{PWAIT}}$	Processor Wait
$\overline{\text{IORQ}}$	Input/Output Request
$\overline{\text{PHOLD}}$	Processor Hold
$\overline{\text{WR}}$	Processor Write
$\overline{\text{RD}}$	Processor Read
$\overline{\text{CCDBS}}/\overline{\text{STADBS}}$	Control and Status Bus Disable
$\overline{\text{MREQ}}$	Memory Request
$\overline{\text{DODBS}}/\overline{\text{ADDBS}}$	Data and Address Bus Disable
$\overline{\text{M1}}$	First State of Instruction Cycle
$\overline{\text{RESET}}$	CPU Reset
$\overline{\text{RFSH}}$	Dynamic Memory Refresh
$\overline{\text{NMI}}$	Non-maskable Interrupt

6.2 DIN CONNECTORS

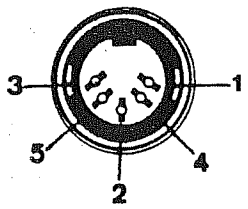
DIN JACK PIN CONNECTIONS FOR EXTERNAL CASSETTE

1 — Remote
2 — Signal Ground
3 — Remote
4 — Input
5 — Output

DIN JACK PIN CONNECTIONS FOR VIDEO INTERFACE

1 — +5V
4 — Video Output
5 — Ground

DIN JACK VIEWED FROM REAR SIDE OF THE GENIE



6.3 INTER-BOARD CONNECTION (CPU – INTERFACE)

PIN	SIGNAL	PIN	SIGNAL
1	CK	17	D0
2	+15V	18	D1
3	PS	19	D5
4	CL	20	D2
5	$\overline{WR}$	21	+5V
6	A11	22	A1
7	CK/2	23	A2
8	$\overline{RD}$	24	A0
9	A10	25	A3
10	VID	26	A5
11	A9	27	A4
12	A8	28	A7
13	D4	29	A6
14	D6	30	$\overline{IN}$
15	D7	31	$\overline{OUT}$
16	D3	32	GND

PS – Page Select
CL – Cassette Local
VID – Video RAM Select

6.4 KEYBOARD – CPU BOARD CONNECTION

PIN	SIGNAL
1	DK4
2	DK6
3	DK3
4	DK7
5	DK5
6	DK2
7	DK0
8	DK1
9	+5V
10	PS
11	CL
12	GND
13	AK0
14	AK1
15	AK2
16	AK3
17	AK4
18	AK5
18	AK5
19	AK6
20	AK7

NOTE: DK4 – buffered data bit 4 and so on.
AK0 – buffered address bit 0 and so on.

6.5 KEYBOARD – NUMERIC KEYPAD CONNECTOR
(GENIE II ONLY)

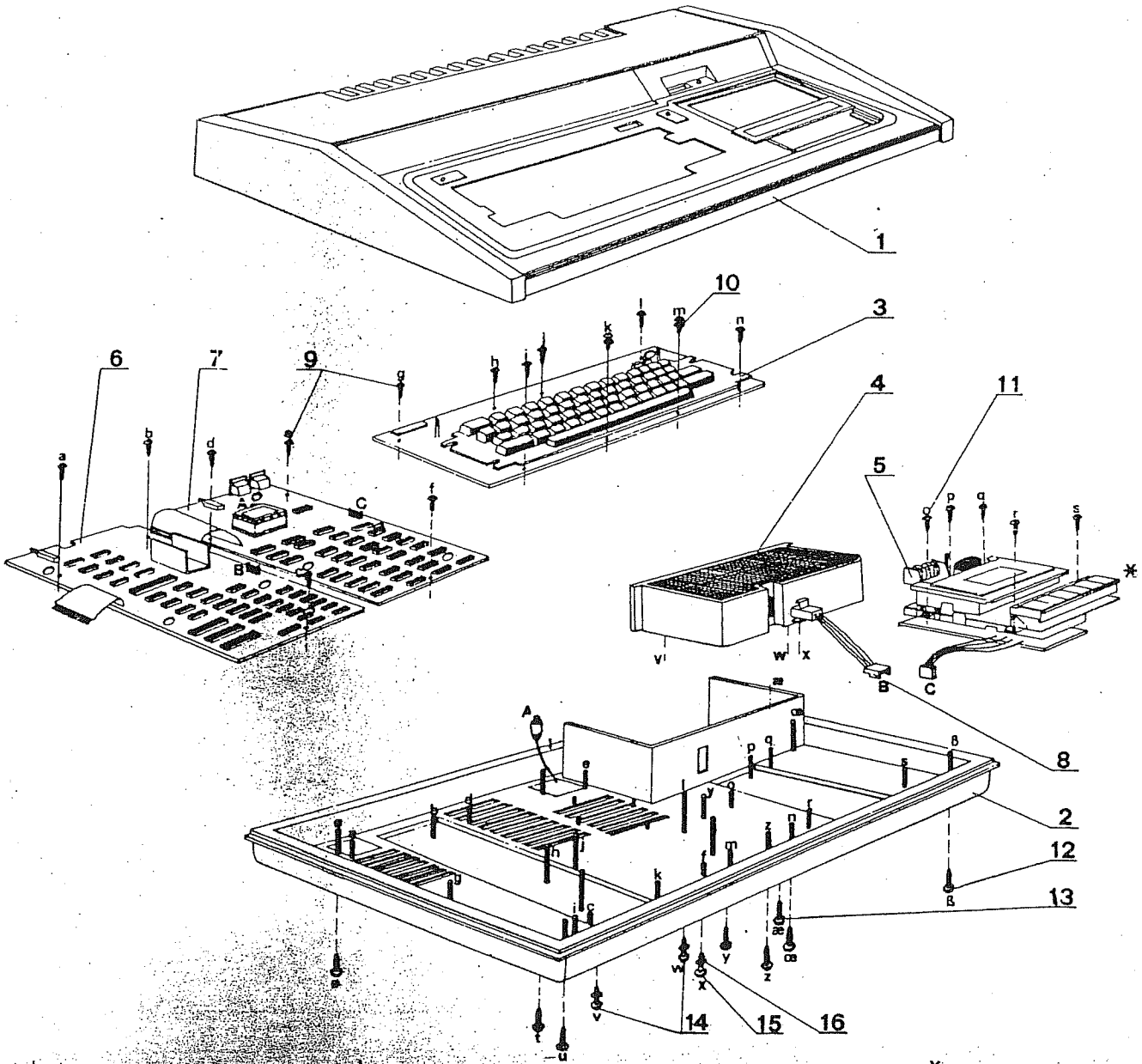
PIN	SIGNAL
1	AK3
2	AK6
3	AK5
4	AK4
5	DK0
6	DK2
7	DK1
8	DK5
9	DK7
10	DK3
11	DK6
12	DK4

7. DISASSEMBLY AND WIRING

In order to disassemble the GENIE, first, unscrew eight screws at the bottom case; 7 around the boundary and 1 at the middle. Second, take off two switch knobs at the back panel. Remove the top case, and you will see the PCB's, power supply and cassette (or numeric keypad in GENIE II) mounted on the bottom case.

After servicing the GENIE, remember to connect up the wires as shown in the wiring diagram.

7.1 DISASSEMBLY DIAGRAM



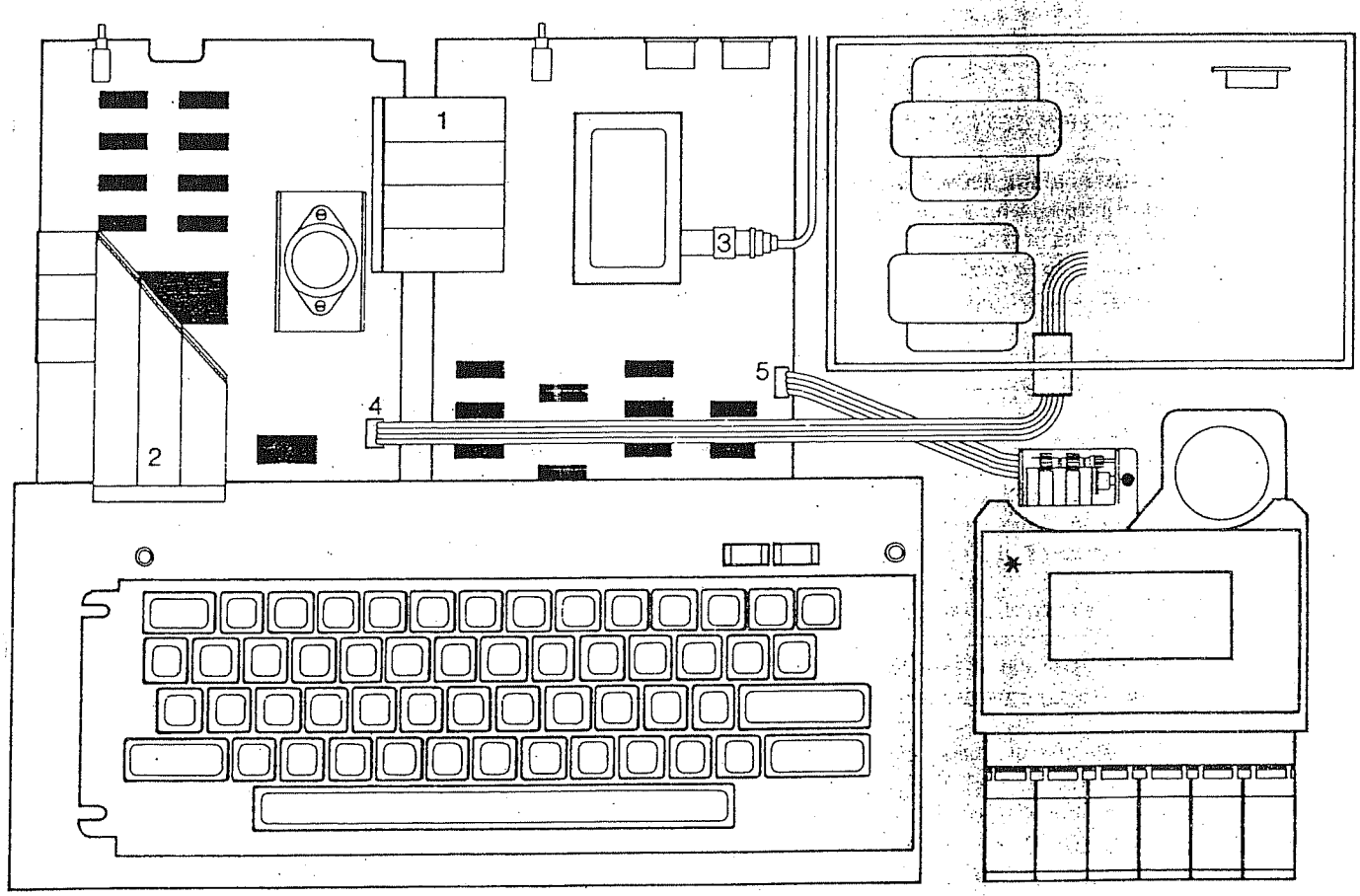
1- TOP CABINET
2- BOTTOM CABINET
3- KEY BOARD
4- POWER SUPPLY UNIT
5- CASSETTE
6- CPU BOARD
7- INTERFACE BOARD
8- POWER SUPPLY CABLE
9- SELF-TAPPING SCREW M3.5x8 (14PCS.)
10- PLAIN WASHER 3.5x0.5x8 (2 PCS.)
11- SELF-TAPPING SCREW M 3 x10 (5PCS.)
12- MACHINE SCREW M 3x0.5 x 30 (7PCS.)
13- MACHINE SCREW M 3x0.5 x 20 (1PCS.)
14- MACHINE SCREW M 3x0.5x22 (1PCS.)
15- MACHINE SCREW M 3x0.5x8 (1PCS.)
16- PLAIN WASHER M 3.5x0.5x6 (3PCS.)

*GENIE I ONLY

ASSEMBLY DIAGRAM

7.2 WIRING DIAGRAM

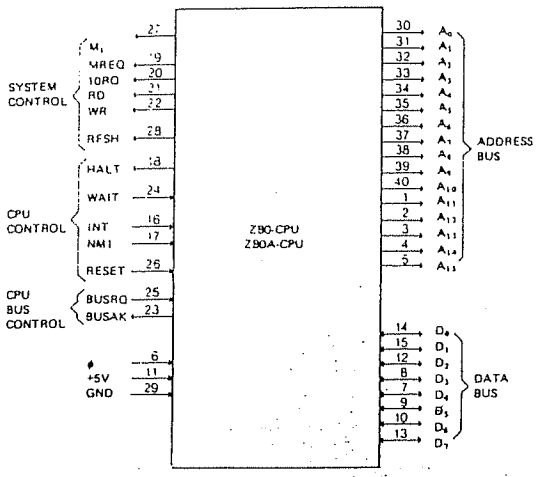
1 – CPU – Interface Interconnection Cable
2 – CPU – Keyboard Interconnection Cable
3 – Antenna Coaxial Cable (TV)
4 – DC Power Connector
5 – Cassette Connector



* Available in GENIE I only
It is replaced by a numeric keypad in GENIE II.

APPENDIX

Z-80 CPU DATA SHEET



Z80, Z80A CPU PIN CONFIGURATION

A_0-A_{15} (Address Bus) — Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.

D_0-D_7 (Data Bus) — Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

$\overline{M_1}$ (Machine Cycle one) — Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.

$\overline{MREQ}$ (Memory Request) — Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$ (Input/ Output Request) — Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

$\overline{RD}$ (Memory Read) — Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$ (Memory Write) — Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$ (Refresh) — Output active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{HALT}$ (Halt state) — Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$ (Wait) — Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.

$\overline{INT}$ (Interrupt Request) — Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.

$\overline{NMI}$ (Non Maskable Interrupt) — Input, active low. The non-maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H.

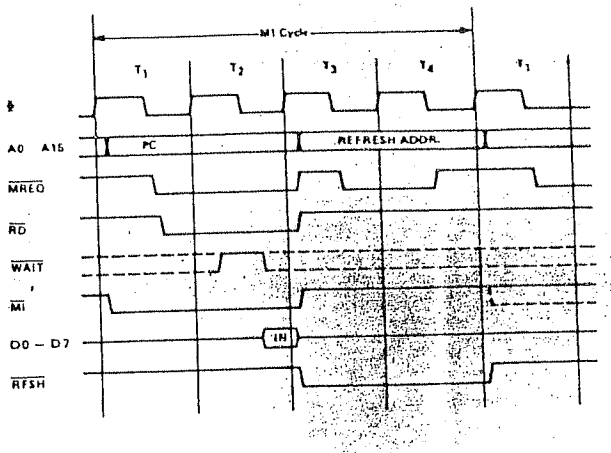
$\overline{RESET}$ — Input, active low. $\overline{RESET}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.

$\overline{BUSRQ}$ (Bus Request) — Input, active low. The bus request signal has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.

$\overline{BUSAK}$ (Bus Acknowledge) — Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these

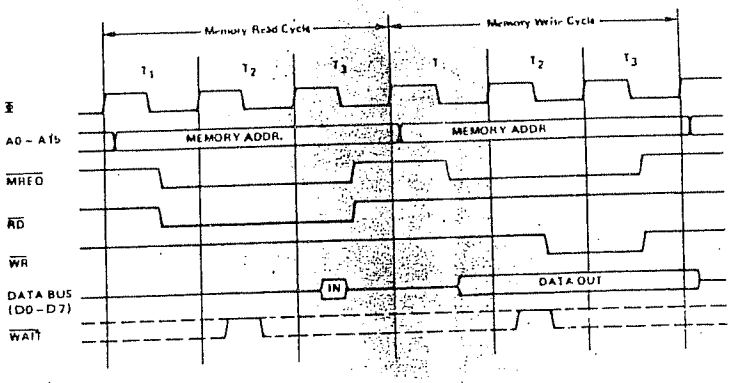
INSTRUCTION OP CODE FETCH

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later MREQ goes active. The falling edge of MREQ can he used directly as a chip enable to dynamic memories. RD when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T_3. Clock states T_3 and T_4 of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The refresh control signal RFSH indicates that a refresh read of all dynamic memories should be accomplished.



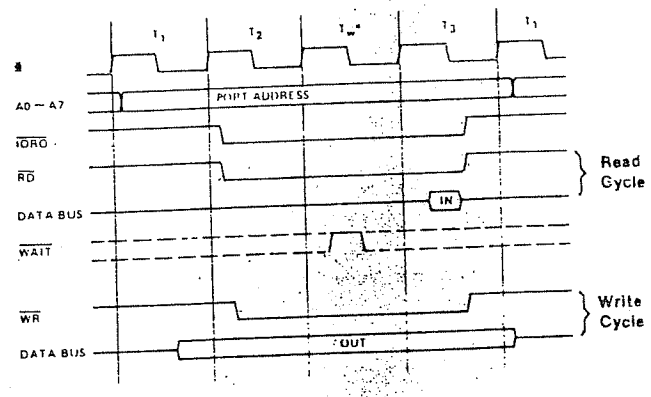
MEMORY READ OR WRITE CYCLES

Illustrated here is the timing of memory read or write cycles other than an OP code fetch (M_1 cycle). The MREQ and RD signals are used exactly as in the fetch cycle. in the case of a memory write cycle, the MREQ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The WR line is active when data on the data bus is stable to that it can be used directly as a R/W pulse on virtually any type of semiconductor memory.



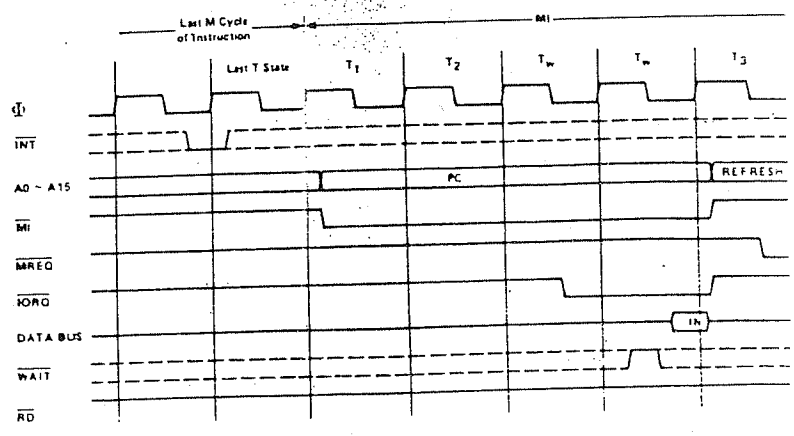
INPUT OR OUTPUT CYCLES

Illustration here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (Tw*). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and active the WAIT line if a wait is required.



INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special M_1 cycle is generated. During this M_1 cycle, the IORQ signal becomes active (instead of MREQ) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the Z80 peripheral controllers, can be easily implemented.



NOTE

EACA INTERNATIONAL LTD
13 Chong Yip Street
Eaca Industrial Building
Kwun Tong, Kowloon, HONG KONG
Telex: 54035 ECHK HX
Cable: "ECHUNG" H.K.
Tels : 3-896323 (8 Lines)

77-4004505-00